

Many-Body Effect and Device Performance Limit of Monolayer InSe

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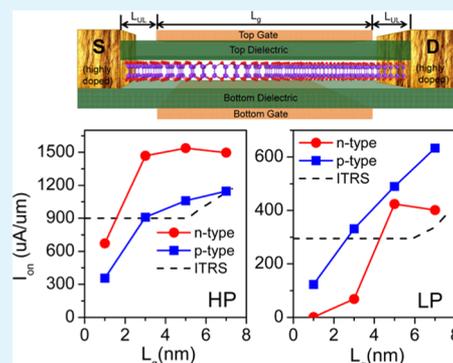
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Supporting Information

ABSTRACT: Due to a higher environmental stability than few-layer black phosphorus and a higher carrier mobility than few-layer dichalcogenides, two-dimensional (2D) semiconductor InSe has become quite a promising channel material for the next-generation field-effect transistors (FETs). Here, we provide the investigation of the many-body effect and transistor performance scaling of monolayer (ML) InSe based on ab initio GW-Bethe–Salpeter equation approaches and quantum transport simulations, respectively. The fundamental band gap of ML InSe is indirect and 2.60 eV. The optical band gap of ML InSe is 2.50 eV for the in-plane polarized light, with the corresponding exciton binding energy of 0.58 eV. The ML InSe metal oxide semiconductor FETs (MOSFETs) show excellent performances with reduced short-channel effects. The on-current, delay time, and dynamic power indicator of the optimized n- and p-type ML InSe MOSFETs can satisfy the high-performance and low-power requirements of the International Technology Roadmap for Semiconductors 2013 both down to 3–5 nm gate length in the ballistic limit. Therefore, a new avenue is opened to continue Moore's law down to 3 nm by utilizing 2D InSe.

KEYWORDS: many-body effect, transistor, sub-10 nm, density functional theory, quantum transport



INTRODUCTION

Scaling of silicon transistors below 5 nm gate lengths (L_g) is predicted to fail because of severe short-channel effects, which means the Moore's law will stop at that point for silicon.^{1–3} The International Technology Roadmap for Semiconductors (ITRS) has proposed that new device architectures and new channel materials are needed to continue the scaling beyond 2020 and 2030, respectively.⁴ Two-dimensional semiconductors (2DSCs) provide a path toward the gate length scaling beyond what is predicted for conventional SCs because they possess several advantages: atomically ultrathin nature allowing excellent gate control, uniform thickness and absence of dangling bonds resulting in decreased interface trap states, and a high degree of vertical scaling.⁵

Currently, the most intensively explored 2D channel materials are transition-metal dichalcogenides (TMDs) like MoS₂^{6–13} and group-VA-ene black phosphorene (BP).^{14–16} TMD field-effect transistors (FETs) are generally quite stable in air, but have a low carrier mobility of a few hundred cm² V⁻¹

s⁻¹, which typically limits the device operating speed and on-current. The sub-10 nm monolayer (ML) MoS₂ FETs is predicted to have a lower on-current that cannot comply with the high-performance (HP) or low-power (LP) requirements of the next decade in the ITRS 2013 by ab initio quantum transport simulations.⁹ Recently, sub-10 nm 2D MoS₂ FETs have been fabricated by several groups, with L_g scaling down to 1 nm¹⁰ or channel length (L_{ch}) scaling down to 4 nm.^{11–13} They all indeed suffer from quite a low maximum current of several to hundred $\mu\text{A}/\mu\text{m}$ and cannot meet the ITRS standards.^{10–13} By contrast, 2D BP has a much higher carrier mobility of 10³ cm² V⁻¹ s⁻¹,¹⁴ and the on-current of sub-10 nm ML BP FETs is predicted to outperform the ITRS HP and LP standards according to ab initio quantum transport simulations (up to 5000 $\mu\text{A}/\mu\text{m}$).^{17,18} However, 2D BP is unstable in air,

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and the devices degrade at ambient condition.¹⁹ Apparently, it is highly desirable to search for a 2DSC with both high carrier mobility/on-current and improved air stability.

2DSC InSe, belonging to the group IIIA monochalcogenide family, has been widely used for optoelectronic applications due to its novel optical properties.^{20–26} However, the investigation on the electronic device applications of 2D InSe is rather limited compared with that on the optoelectronic ones. 2D InSe FETs have a high electron mobility exceeding $10^3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$,^{27–30} which is much higher than that in MoS_2 FETs and comparable to that in BP FETs. Remarkably, they are quite stable without the ambient degradation in air.^{29,31} The two virtues collectively render 2D InSe a competitive channel for the next-generation FETs.²⁹ The scale length λ is defined as $\lambda = \sqrt{t_{\text{ch}} t_{\text{ox}} \epsilon_{\text{ch}} / \epsilon_{\text{ox}}}$, where $t_{\text{ch/ox}}$ and $\epsilon_{\text{ch/ox}}$ are the thickness and dielectric constant of the channel/gate oxide, respectively. A ML channel region has a shorter scale length and is always desirable to suppress the short-channel effects. The hBN-sandwiched ML InSe FETs have been fabricated with few-layer graphene as electrodes. However, the device yields a low current on/off ratio of only 10^2 , limited by the high electrode contact resistances and interface scattering.²⁹ The performance limit of an intrinsic ML InSe FET remains unknown. The sub-10 nm 2D InSe FETs can be fabricated following the same technique used to fabricate sub-10 nm MoS_2 FETs. It is important to provide a prediction before an experimental fabrication to answer whether they can meet the ITRS HP or LP requirements for the next decade or even beyond.

In this article, we investigate the many-body effect of ML InSe and the performance limit of n- and p-type ML InSe FETs scaling down to 1 nm gate length using ab initio GW and GW-Bethe–Salpeter equation (BSE) approaches and quantum transport simulations, respectively. The calculated indirect fundamental band gap of ML InSe is 2.60 eV. The optical band gap is 2.50 eV for the in-plane polarized light, which is comparable with the observed lowest energy photoluminescence peak (~ 2.9 eV),²⁹ with the corresponding exciton binding energy of 0.58 eV. The simulated sub-7 nm- L_g double-gated (DG) ML InSe metal oxide semiconductor FETs (MOSFETs) show device performances superior to ML MoS_2 . Both n- and p-type ML InSe MOSFETs are able to be scaled down to 3 nm for HP applications and down to 5 and 3 nm for LP applications, respectively, in terms of the calculated on-current, delay time, and dynamic power indicator in the ballistic limit, all of which surpass the standards of ITRS 2013 for the 2028 horizon. Hence, 2D InSe is a competitive channel for the next-generation FETs.

COMPUTATIONAL METHODS

The geometry optimizations are based on the density functional theory (DFT) performed with the projector-augmented wave pseudopotential and plane-wave basis set with a cutoff energy of 400 eV implemented in the Vienna ab initio simulation package.³² The generalized gradient approximation (GGA) with the Perdew–Burke–Ernzerhof (PBE) functional is adopted. A vacuum space above 15 Å is chosen to eliminate the spurious interaction between periodic images. The k-point mesh is sampled with $13 \times 13 \times 1$ for the structure relaxation. The energy difference is converged to 10^{-5} eV/atom and the maximum residual force is converged to 0.01 eV/Å. The electronic band calculation is performed subsequently with GGA and Heyd–Scuseria–Ernzerhof (HSE) hybrid functionals, respectively, using a triple denser k-point mesh ($36 \times 36 \times 1$).

The quasiparticle calculations are performed with the BerkeleyGW package.³³ The quasiparticle energies E_{nk} are obtained within the GW approximation by solving the Dyson equation³⁴

$$\left[H_0 + \sum (E_{\text{nk}}) \right] \Psi_{\text{nk}} = E_{\text{nk}} \Psi_{\text{nk}} \quad (1)$$

where H_0 is the Hamiltonian in the Hartree approximation, \sum is the electron self-energy, and Ψ_{nk} is the quasiparticle wave function. The quasiparticle wave functions are assumed to be same as the DFT wave functions, which are obtained by performing mean-field calculations using the GGA functional in the Troullier–Martins norm-conserving pseudopotential scheme in the Quantum Espresso code.³⁵ The kinetic energy cutoff is 70 Ry. The k-point mesh is sampled with $24 \times 24 \times 1$. To calculate the excitation spectrum, we solve the BSE on a $72 \times 72 \times 1$ k-grid (see the Supporting Information Section 1 for details).

The device simulations are performed in the ATK 2016 package³⁶ using the DFT coupled with the nonequilibrium Green's function (NEGF) method with double- ζ -polarized basis set. GGA of the PBE form is adopted. In a device configuration, ML InSe is either heavily doped in the source/drain region or doped by the dual gates. In this case, self-energy corrections and thereby the quasiparticle band gap are greatly reduced due to the significant screening by doping carriers,³⁷ and the DFT–GGA band gap is comparable with the quasiparticle GW band gap. For example, the calculated band gaps of degenerately doped MoSe_2 at the GGA–PBE and GW levels are 1.43 and 1.59 eV, respectively,^{38,39} both of which are close to the observed value of 1.58 eV.⁴⁰ Therefore, GGA–PBE is expected to give a good approximation of the experimental transport gap. One example is ML phosphorene, whose GGA–PBE band gap is 0.91 eV and measured transport gap is 1.0 eV.^{41,42} The difference between the DFT–GGA band gap and experimental value are within 10% in the doping cases. The 10% underestimation of the transport gap may lead to a slight increase in the current.

The ML InSe channel is enclosed in a bounding box and located in the xz -plane. The transport is along the z -direction. The electrostatic potential is defined on a regular grid inside the bounding box calculated from the Poisson equation. Neumann boundary condition is adopted for the y -direction, that is, the electric field is zero at the boundary. Periodic boundary condition is used for the x -direction. Dirichlet boundary condition is used for the z -direction, where the electrostatic potential is determined by the potential of the semi-infinite electrodes. The dual gates and dielectric oxides are added by including an electrostatic interaction with a continuum of metallic or dielectric material inside the bounding box. The k-point meshes for the central region and electrodes are sampled with $50 \times 1 \times 1$ and $50 \times 1 \times 50$, respectively. The transmission coefficient at k_x point and energy E is obtained by

$$T(k_x, E) = \text{Tr}[\Gamma_L(k_x, E) G^r(k_x, E) G^a(k_x, E) \Gamma_R(k_x, E)] \quad (2)$$

where $G^{r(a)}$ is the retarded (advanced) Green function and $\Gamma_{L(R)}(k_x, E) = i(\sum_{L(R)}^a(k_x, E) - \sum_{L(R)}^r(k_x, E))$ is the level broadening due to left (right) electrode expressed in terms of the electrode self-energy $\sum_{L(R)}^a(k_x, E)$. The transmission function at a given energy $T(E)$ is averaged over 50 k_x -points in the irreducible Brillouin zone. The drain current is calculated with the Landauer–Büttiker formula⁴³

$$I_d(V_{\text{ds}}, V_g) = \frac{2e}{h} \int_{-\infty}^{+\infty} \{ T(E, V_{\text{ds}}, V_g) [f_S(E - \mu_S) - f_D(E - \mu_D)] \} dE \quad (3)$$

where $T(E, V_{\text{ds}}, V_g)$ is the transmission probability at a given gate voltage V_g and bias voltage V_{ds} , $f_{S/D}$ is the Fermi–Dirac distribution function for the source/drain electrode, and μ_S/μ_D is the electrochemical potential of the source/drain electrode. The temperature is set to 300 K.

RESULTS AND DISCUSSION

Basic Electrical and Optical Properties. ML InSe has a honeycomb lattice that consists of four covalently bonded Se–

In–In–Se atomic planes (see Figure 1a). The optimized lattice constant (a) and Se–Se height (h) of ML InSe are 4.095 and

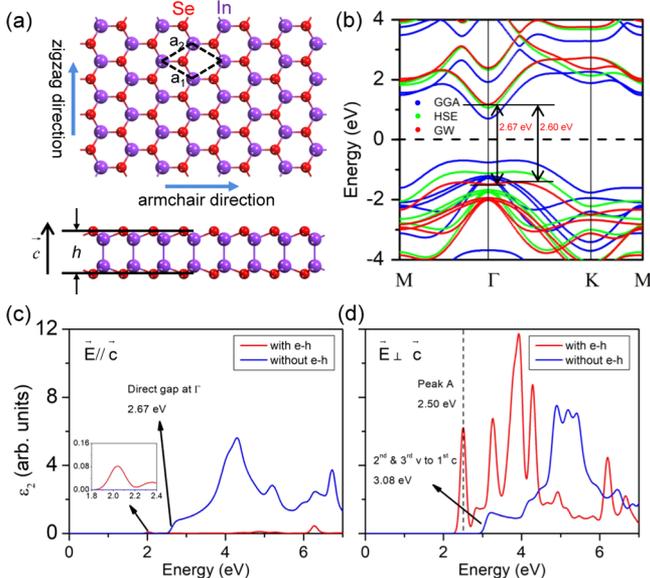


Figure 1. (a) Schematic of the ML InSe crystal structure. (b) Band structures of ML InSe calculated with GGA, HSE, and GW approaches, respectively. (c, d) Imaginary part ϵ_2 of dielectric function of ML InSe with and without the e–h interaction for $\vec{E} \parallel \vec{c}$ (out-of-plane) polarization (c) and $\vec{E} \perp \vec{c}$ (in-plane) polarization (d).

4.729 Å, respectively. The band structures of ML InSe using GGA, HSE, and GW approaches are compared in Figure 1b. An indirect band gap is always observed in ML InSe. It is 1.40 eV at the GGA level, which is consistent with the previous values (1.40–1.44 eV).^{29,44} The indirect band gap is 2.14 eV at the HSE level and increases significantly to 2.60 eV at the GW level. The direct GW band gap at Γ point is 2.67 eV. The GW method can well reproduce the fundamental (quasiparticle) band gap of 2DSCs by including the electron–electron interaction in terms of the self-energy operator, whereas the HSE method closely relies on the empirical choice of the percentage of the Hartree–Fock interaction matrix and the screening length of short-range electron–electron interactions and often gives a gap lying between the GW and GGA values in 2DSCs.⁵⁷ The conduction band is much more flat than the valence band in ML InSe. The corresponding electron and hole effective masses (m_e^* and m_h^*) of ML InSe differ by 1 order of magnitude with $m_e^* \sim 0.24m_0$ and $m_h^* \sim 2.6m_0$ (m_0 is bare electron mass), which are of negligible anisotropy along the zigzag and armchair directions.

The calculated optical spectra of ML InSe with and without the excitonic effects are shown in Figure 1c,d for both out-of-plane and in-plane polarization directions, respectively. Because of the mirror-plane symmetry in ML InSe, only the transitions between the bands of different symmetries are allowed for out-of-plane polarization, whereas only the transitions between the bands of the same parity are allowed for in-plane polarization. The parities of the valence and conduction edges are different with respect to the mirror transformation. Therefore, the lowest-energy transition is active for the out-of-plane polarized light (Figure 1c). The optical absorption edge is located at 2.67 eV without the e–h interaction, corresponding to the direct electronic GW gap at the Γ point. The light-absorption intensity is greatly sup-

pressed for the out-of-plane polarized light after considering the e–h interaction due to the ultrathin thickness of ML InSe, with a negligible peak located at 2.04 eV. The transition between the two deeper valence bands and the lowest conduction band is permitted for in-plane polarization owing to the same parity (Figure 1d) and has an absorption edge at ~ 3.08 eV without the e–h interaction. After the inclusion of the e–h interaction, the optical spectrum shows an absorption peak A at 2.50 eV, which is comparable with the observed lowest-energy photoluminescence peak (~ 2.9 eV) in ML InSe.²⁹

We define the binding energy of peak A exciton as the relative energy difference between peak A and second/third-valence to the first conduction band gap (3.08 eV), i.e., 0.58 eV, which is comparable with or slightly smaller than those in other 2DSCs, such as ML graphdiyne (0.55 eV),⁴⁵ ML group-VA-enes BP, arsenene, and antimonene (0.8–0.9 eV),^{36,37,46} and ML MoS₂ (~ 1.0 eV).⁴⁷ The real-space wave functions for peak A bound exciton are provided in the Supporting Information Section 1 Figure S3 obtained by fixing the position of the hole in the center of supercells. The envelopes of such exciton wave functions are nearly like $2p_x$ and $2p_y$ states in a 2D hydrogenic model. The first exciton peak position located at 2.04 eV is a dark exciton state, resembling the $1s$ state in a 2D hydrogenic model.

DG ML InSe MOSFETs. A DG two-probe model is used to calculate the ballistic transport properties of the ML InSe MOSFETs (Figure 2a). Symmetric underlap (UL) structure,

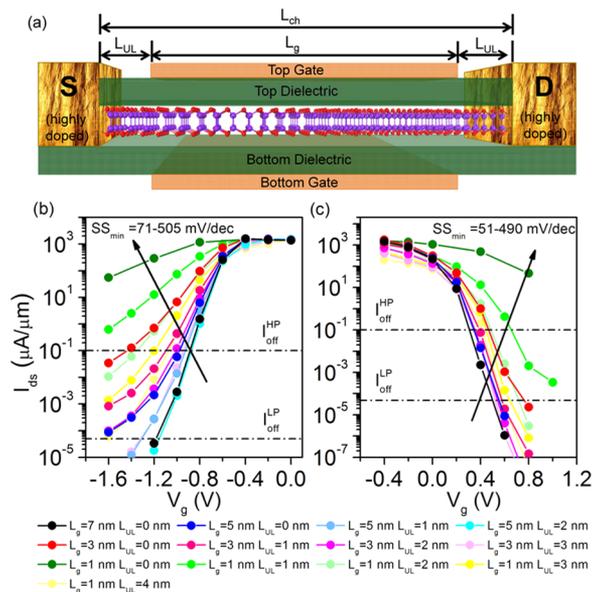


Figure 2. DG ML InSe MOSFET. (a) Schematic of the device structure. (b, c) Transfer characteristics for the n- (b) and p-type (c) devices at different L_g and L_{UL} as indicated by the legend below. $V_{ds} = 0.64$ V is adopted for all our simulations. Dot-dashed lines represent the I_{off} required by the ITRS 2013 for the 5.1 nm HP and 5.9 nm LP devices at the 2028 horizon.

i.e., ungated section of the channel at both source and drain ends, is also considered in the n-type ML InSe MOSFETs with $L_g \leq 5$ nm and in the p-type ones with $L_g \leq 3$ nm; meanwhile, the whole channel length ($=L_g + 2L_{UL}$) does not exceed 9 nm. It is critical to adopt an appropriate electron/hole doping concentration ($N_{e/h}$) in the source and drain regions of a

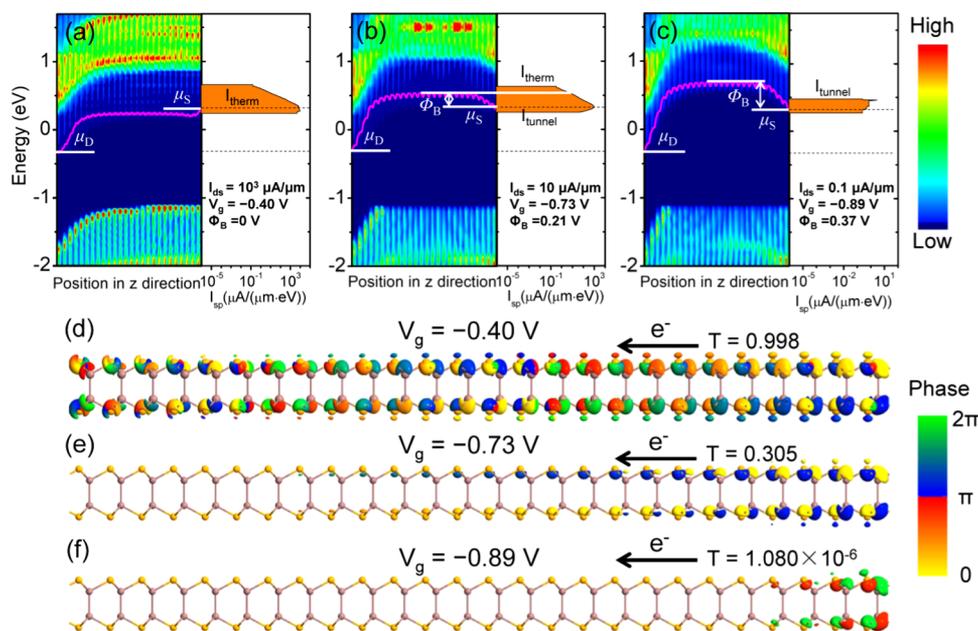


Figure 3. (a–c) Position-resolved local density of states (LDOS) in the channel region and spectral current density for the n-type 7 nm- L_g DG ML InSe MOSFETs at $I_{ds} = 10^3$ (a), 10 (b), and $0.1 \mu\text{A}/\mu\text{m}$ (c), respectively. The responding conduction band profiles along the channel are represented by magenta lines. μ_s and μ_d are the electrochemical potentials of the source and drain, respectively. Φ_B is the effective barrier height. The spectral current densities are given in the logarithmic scale. The contributions from the thermionic and tunneling transports (I_{therm} and I_{tunnel}) are illustrated. (d–f) Conductance eigenchannels at $(\mathbf{k}, E) = (\Gamma, 0.32 \text{ eV})$ for $V_g = -0.40, -0.73,$ and -0.89 V , respectively. The isovalue is 0.2 au .

MOSFET to achieve the optimal performance. Therefore, a coarse $N_{e/h}$ -dependent study of the device transfer characteristics is provided in the Supporting Information Section 2. Among our studied $N_{e/h}$, N_e of 10^{13} cm^{-2} and N_h of $9 \times 10^{13} \text{ cm}^{-2}$ are optimum for the n- and p-type ML InSe MOSFETs, respectively. Because there is no standard for the sub-5 nm nodes by the ITRS 2013, the figures of merit for the sub-5 nm MOSFETs are benchmarked with the requirements of the shortest 5.1 nm-HP or 5.9 nm-LP device in the ITRS 2013 for the 2028 horizon. The equivalent oxide thickness of 0.41 nm and V_{ds} of 0.64 V are adopted for all the investigated MOSFETs according to the ITRS standards for 2028. On-current is evaluated under a supply voltage ($V_{dd} = V_{ds}$) of 0.64 V, with the off-current fixed at the ITRS requirements, namely, $I_{off} = 0.1 \mu\text{A}/\mu\text{m}$ for all the HP devices and $I_{off} = 4 \times 10^{-5}$ and $5 \times 10^{-5} \mu\text{A}/\mu\text{m}$ for the 7 nm- L_g and sub-5 nm- L_g LP devices, respectively.

The transfer characteristics of the n- and p-type ML InSe MOSFETs with different L_g and L_{UL} are presented in Figure 2b,c, respectively. To illustrate the gate modulation mechanism, the device local density of states (LDOS) and spectral current density (I_{sp}) of the n-type 7 nm- L_g ML InSe MOSFET at $I_{ds} = 10^3, 10$ and $0.1 \mu\text{A}/\mu\text{m}$ are provided in Figure 3a–c as an example. This device achieves I_{ds} of $10^3 \mu\text{A}/\mu\text{m}$ at $V_g = -0.40 \text{ V}$, and the corresponding barrier height Φ_B is zero (Figure 3a). Thermionic emission dominates the electron transport. To reduce the current by 2 and 4 orders of magnitude, V_g needs to be decreased to -0.73 and -0.89 V and the corresponding Φ_B increased to 0.21 and 0.37 V (Figure 3b,c), respectively. The transport by thermionic emission is greatly suppressed, and the contribution from electron tunneling is observed at $I_{ds} = 10 \mu\text{A}/\mu\text{m}$. At $I_{ds} = 0.1 \mu\text{A}/\mu\text{m}$, tunneling becomes the main contribution. The corresponding eigenchannel analysis is also provided in Figure 3d–f. The eigenchannel at $(\mathbf{k}, E) = (\Gamma, 0.32 \text{ eV})$ for $V_g =$

-0.40 V has almost 100% transmission, exhibiting a full-phase oscillation and a uniform electron density. In contrast, the eigenchannels have only 30.5% and near 0 transmission for $V_g = -0.73$ and -0.89 V , respectively, with the rest of the electron wavepacket backscattered, leading to a partial standing wave on the right with the phase of almost pure real ($0/2\pi$) and imaginary (π).

The steepest subthreshold swing (SS_{min}), averaged SS (SS_{avg}), and on-current of the two groups of the $I_{ds}-V_g$ curves in Figure 2b,c are derived and plotted as a function of L_{UL} , as shown in Figure 4. SS_{avg} is averaged over one decade of drain current for the $L_g = 1 \text{ nm}$ and $L_{UL} = 0$ cases and over three decades of drain current for the remaining cases. We first concentrate on the $L_{UL} = 0$ cases. In the n-type devices without a UL structure, SS_{min} is 71 mV/dec and SS_{avg} is 80 mV/dec at $L_g = 7 \text{ nm}$, which are comparable with the value of 80 mV/dec at $L_g = 6 \text{ nm}$ reported by Ahn and Shin based on the ab initio quantum transport simulations.⁴⁸ And, SS_{min} and SS_{avg} rapidly rise to 505 and 619 mV/dec, respectively, as L_g decreases to 1 nm. Therefore, an increased $|V_{g(off)} - V_{th}|$ is needed to achieve the ITRS requirement for the off-current as L_g decreases, which inevitably limits the overdrive voltage $|V_{g(on)} - V_{th}|$ and hence lowers the on-current. I_{on} of the n-type ML InSe HP device is 1497, 1538, and $107 \mu\text{A}/\mu\text{m}$, respectively, at $L_g = 7, 5,$ and 3 nm without the UL structure (Table 1 and Figure 4c). The former two devices can fulfill the ITRS on-current requirement (1100 and $900 \mu\text{A}/\mu\text{m}$ for the 6.7 and 5.1 nm- L_g HP devices, respectively), but the 3 nm one apparently cannot fulfill the ITRS on-current requirement at the 5.1 nm node. $V_{g(off)}$ of the 1 nm- L_g HP device without a UL is beyond our studied gating range as shown in Figure 2b because of the large SS and thereby incredibly large $|V_{g(off)} - V_{th}|$. For the LP applications, only the 7 nm- L_g n-type ML InSe MOSFET can satisfy the extremely small I_{off} required by the ITRS without the aid of a UL structure and has an I_{on} of $401 \mu\text{A}/\mu\text{m}$, which

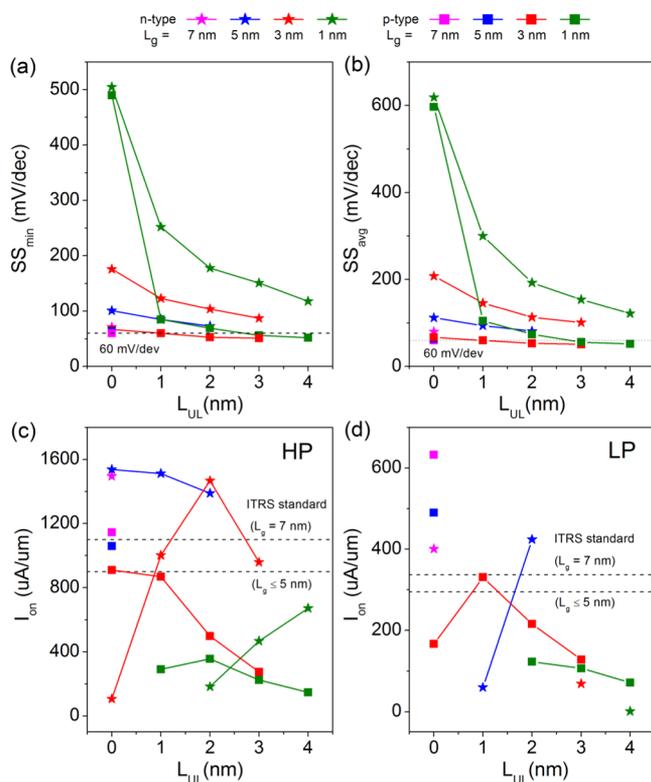


Figure 4. (a) SS_{min} , (b) SS_{avg} , (c) HP- I_{on} , and (d) LP- I_{on} versus L_{UL} for the n- and p-type ML InSe MOSFETs at different L_g as indicated in the legend above. Black dashed line in (a) and (b) indicates the Boltzmann limit of 60 mV/dec for SS at room temperature and in (c) and (d) represents the ITRS HP/LP requirements for $L_g = 7$ nm and ≤ 5 nm.

overruns the ITRS LP device standard of 337 $\mu A/\mu m$ (Table 1 and Figure 4d).

For the p-type devices without UL, SS_{min} and SS_{avg} are 60 mV/dec at $L_g = 7$ nm and increase to 490 and 597 mV/dec, respectively, at $L_g = 1$ nm, smaller than those of the n-type FETs at the same L_g (Figure 4a,b). I_{on} of the p-type ML InSe 7-, 5-, and 3-nm- L_g HP devices and 7- and 5-nm- L_g LP devices are all able to satisfy the corresponding ITRS requirements at $L_{UL} = 0$ (Table 1 and Figure 4c,d). The 3-nm- L_g ML InSe LP MOSFET without a UL only can meet 60% of the ITRS on-current requirement at the 5.9 nm node. $V_{g(off)}$ of both HP and LP devices is beyond our studied gating range at $L_g = 1$ nm and $L_{UL} = 0$ because of the large SS. In one word, the n-type ML InSe MOSFETs without a UL structure can satisfy the ITRS HP and LP requirements down to 5 and 7 nm, respectively, whereas the p-type ML InSe MOSFETs can satisfy the ITRS HP and LP requirements down to smaller 3 and 5 nm, respectively.

The UL structure in the source/drain side can be used to improve the immunity to the short-channel effects in MOSFET devices, as it increases the effective channel length and suppresses the source–drain tunneling (Supporting Information Section 3). After introducing the UL structures, SS is always improved with the increasing L_{UL} irrespective of L_g (Figure 4a,b). Some SSs are even below 60 mV/dec in the p-type devices. This steep sub-60 mV/dec switching characteristic is caused by the tunneling component beside the thermionic current. Although the UL structure improves SS, the current in the superthreshold region is greatly degraded by

the UL, and it is particularly obvious in the p-type case (see the Supporting Information Section 3).

As the UL structure improves SS but lowers the current in the superthreshold region, no UL is needed for the long-gate-length devices because their SS is low enough (7-nm- L_g n-type and 7- and 5-nm- L_g p-type devices). But appropriate L_{UL} is preferred in the shorter-gate-length devices in terms of I_{on} . As shown in Figure 4c,d, the optimum I_{on} is achieved at $L_{UL} = 0$ (2), 2 (3), and 4 (4) nm, respectively, for the n-type 5-, 3-, and 1-nm- L_g ML InSe HP (LP) MOSFET and at $L_{UL} = 0$ (1) and 2 (2) nm, respectively, for the p-type 3- and 1-nm- L_g ML InSe HP (LP) MOSFET. Moreover, I_{on} appears to be further boosted as L_{UL} continues to increase for the n-type 1-nm- L_g HP devices and all n-type LP devices according to the tendency.

Figure 5 presents the optimal I_{on} of the ML InSe HP and LP MOSFETs at different L_g . With the assistance of the UL design, the gate length of the n-type ML InSe MOSFETs that satisfy the ITRS HP/LP requirements is reduced from 5/7 to 3/5 nm, and the gate length of the p-type ML InSe MOSFETs that satisfy the ITRS LP requirements is reduced from 5 to 3 nm. In terms of the optimal on-current, the n-type ML InSe MOSFETs are more suitable for HP applications, whereas the p-type ones are more suitable for the LP applications. The reason can be ascribed to the different electron and hole effective masses in ML InSe. The smaller electron effective mass m_e^* ($\sim 0.24m_0$) in ML InSe leads to a faster carrier velocity because $v = \frac{1}{\hbar} \frac{dE}{dk} = \frac{\hbar k}{m^*}$, and hence a higher current drive capability, so n-type ML InSe MOSFETs have a higher I_{on} and thus a smaller delay time, as required by HP devices. On the other hand, the larger hole effective mass m_h^* ($\sim 2.6m_0$) suppresses the source–drain direct tunneling leakage because $T \propto e^{-l\sqrt{m^*\Phi_B}}$, where l is the barrier width. Therefore, a much smaller leakage current and a much steeper SS are achieved in the p-type ML InSe MOSFETs, as preferred by LP devices. The L_g -dependence of other device electrical properties, like intrinsic gate capacitance C_g , quantum capacitance C_Q , transconductance g_m , and field-effect mobility μ_{FE} , is also studied (see the Supporting Information Section 4).

The intrinsic gate delay time τ and power dissipation (PDP) per device width (dynamic power indicator) are another two important parameters for MOSFETs. The delay time τ provides a frequency limitation and PDP reflects the power efficiency for the transistor operation. The calculated delay time $\tau = \frac{C_g V_{dd}}{I_{on}}$ of the optimized ML InSe MOSFETs is 0.016–0.294/0.070–9.449 (HP/LP) ps as listed in Table 1, smaller than the ITRS standards of 0.423–0.446/1.493–1.514 (HP/LP) ps, except the $L_g = 1$ nm and $L_{UL} = 4$ nm cases, indicating the ability to handle a rapid operation. According to the equation $PDP = (Q_{on} - Q_{off})V_{ds}/W$, where Q_{on} and Q_{off} are the total charges of the channel in the on and off states, respectively, PDP of the ML InSe MOSFETs is 0.006–0.049 fJ/ μm and generally increases with the increasing L_g . Compared with the ITRS requirements (0.24–0.34 fJ/ μm), ML InSe devices cost much less energy during the switching. Therefore, ML InSe FETs are capable of achieving low delay and low energy simultaneously.

The source and drain are degenerately doped in the channel itself in MOSFETs, and no Schottky barrier exists between the source/drain and channel. Due to the lack of a sustainable doping scheme in 2DSC devices, metal electrodes are generally

Table 1. Benchmark of the Ballistic Performance Upper Limits of the Optimized ML InSe DG n- and p-Type MOSFETs against the ITRS 2013 Requirements for HP and LP Devices of the Next Decades^a

	L_g (nm)	L_{UL} (nm)	SS_{min} (mV/dec)	SS_{avg} (mV/dec)	I_{off} ($\mu A/\mu m$)	I_{on} ($\mu A/\mu m$)	I_{on}/I_{off}	τ (ps)	PDP (fJ/ μm)
n-type ^b HP	7	0	71	80	0.1	1497	1.50×10^4	0.030	0.032
	5	0	101	112	0.1	1538	1.54×10^4	0.025	0.026
	3	0	176	208	0.1	107	1.07×10^3	0.294	0.022
	1	0	505	619	^d	1468	1.47×10^4	0.016	0.013
n-type ^b LP	7	0	71	80	4×10^{-5}	401	1.00×10^7	0.112	0.026
	5	0	101	112	^d				
	3	0	176	208	5×10^{-5}	424	8.48×10^6	0.070	0.013
	1	0	505	619	^d				
p-type ^c HP	7	0	60	60	0.1	1146	1.05×10^4	0.054	0.049
	5	0	64	64	0.1	1060	1.06×10^4	0.051	0.038
	3	0	67	67	0.1	910	9.10×10^3	0.041	0.027
	1	0	490	597	^d				
p-type ^c LP	7	0	60	60	4×10^{-5}	633	1.58×10^7	0.098	0.043
	5	0	64	64	5×10^{-5}	490	9.8×10^6	0.111	0.034
	3	0	67	67	5×10^{-5}	167	3.34×10^6	0.223	0.021
	1	0	60	60	5×10^{-5}	331	6.62×10^6	0.084	0.017
		2	69	74	5×10^{-5}	123	2.46×10^6	0.110	0.007
ITRS HP 2025	6.7				0.1	1100	1.10×10^4	0.446	0.33
ITRS HP 2028	5.1				0.1	900	9.00×10^3	0.423	0.24
ITRS LP 2026	7.0				4×10^{-5}	337	8.43×10^{-6}	1.514	0.34
ITRS LP 2028	5.9				5×10^{-5}	295	5.90×10^6	1.493	0.28

^a SS_{min} : the steepest subthreshold swing; SS_{avg} : the averaged subthreshold swing; τ : delay time; PDP: power dissipation. ^bData for the optimized n-type devices at $N_e = 10^{13} \text{ cm}^{-2}$. ^cData for the optimized p-type devices at $N_e = 9 \times 10^{13} \text{ cm}^{-2}$ under a fixed $V_{ds} = 0.64 \text{ V}$. ^dITRS I_{off} standard cannot be reached in our investigate gate voltage region.

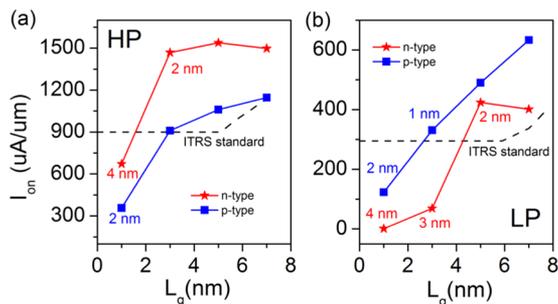


Figure 5. On-current versus the gate length of the optimized n- and p-type ML InSe HP (a) and LP (b) MOSFETs. The length of UL is indicated, otherwise $L_{UL} = 0$. Black dashed lines represent the ITRS standards.

used and usually lead to a large contact resistance arising from the formation of Schottky barriers.⁴⁹ For example, the fabricated ML InSe FETs with few-layer graphene as electrodes exhibit resistances larger than $1 \text{ M}\Omega$, which strongly degrade their performances.²⁹ An Ohmic contact is highly desired to lower the contact resistance, otherwise the intrinsic high performance of ML InSe devices will be masked by the low contact quality of the electrodes. Luckily, Cu electrode is predicted to form a n-type Ohmic contact with ML InSe according to ab initio electronic calculations and quantum transport simulations.⁵⁰ It is relatively difficult to realize an Ohmic p-type contact with ML InSe considering its large band

gap, high work function, and high optimal hole doping density. The O-terminated MXenes may serve as a good option because some of them have quite high work functions up to 8 eV ⁵¹ and the van der Waals interaction with 2D InSe can lead to a weak Fermi level pinning.

It can be noted that ML isoelectronic GaS, GaSe, and InS share similar electronic properties with ML InSe. Therefore, they could also be applied for sub-5 nm logical devices with appropriate electrodes. The p-type DG ML GaSe MOSFET has been simulated in the sub-5 nm range. The on-currents of the 3- and 5 nm- L_g p-type DG ML GaSe MOSFETs are around $1700 \mu A/\mu m$, which are slightly larger than those of the ML InSe ones at the same gate length (910 and $1060 \mu A/\mu m$, respectively).⁵² SS of the p-type DG MOSFET based on ML GaSe is around 60 mV/dec at $L_g = 4$ and 5 nm and increases to 92 mV/dec at $L_g = 3 \text{ nm}$.⁵² By contrast, SSs of the p-type DG ML InSe MOSFETs are all close to 60 mV/dec at 3–5 nm gate lengths. Hence, the short-channel effect is more insignificant in the ML InSe MOSFETs in terms of SS. We also compare the transfer characteristics of the DG ML InSe MOSFETs with the DG ML MoS₂ and BP FETs at the ultimate gate length (Supporting Information Section 5). The ML InSe devices are superior to the MoS₂ ones in terms of the larger on-current and superior to the BP ones in terms of the higher stability.

We also estimate the reliability of our ab initio DFT–NEGF transport simulations by comparing the simulated and

experimental transfer characteristics of the 1 nm- L_g 2D MoS₂ transistor in the Supporting Information Section 6.¹⁰ Our simulation well reproduces the experimental transfer characteristic of the 1 nm- L_g 2D MoS₂ transistor in the subthreshold regime, with the calculated and observed SS of 66 and 65 mV/dec, respectively. The simulated maximum current is several times larger than the experimental one. This discrepancy is caused by the fact that our simulated MOSFET is adopted with Ohmic contact and ballistic transport features, whereas the experimental MoS₂ FET may have Schottky barrier as the adopting metal Ni electrodes and inevitably suffer lattice phonon and interfacial Coulomb scatterings. All the factors decrease the maximum current. A proper metal contact can lead to the formation of Ohmic contact with ML InSe.⁵⁰ The phonon scattering is weak when the channel length is scaled down to sub-7 nm. A high ballisticity of at least 80% has been proved in the sub-7 nm ML MoS₂ and BP MOSFETs, which is defined as the current ratio between the phonon scattering case and the purely ballistic case.^{53,54} The interfacial Coulomb scattering is left as the main concern. The carrier scattering from interfacial Coulomb impurities (e.g., chemical residues surface dangling bonds, and gaseous adsorbates) will be greatly intensified in ML channel because of the close proximity between carriers and impurities, resulting in low carrier mobility.⁵⁵ Some measures can be taken to improve the interface quality and mitigate the interface scattering in transistors, such as vacuum annealing and adopting 2D dangling bond free dielectrics,^{56,57} which would lead to rational performance improvement. Our simulation provides an upper performance limit of the n- and p-type ML InSe MOSFETs. By adopting Ohmic contact electrode and improving the surface quality, we believe the limit can be gradually approached.

CONCLUSIONS

We provide the first investigation of the fundamental and optical band gaps of ML InSe from GW and GW-BSE approaches and the performance limit of both n- and p-type ML InSe MOSFETs based on the ab initio quantum transport simulations. ML InSe has an indirect GW band gap of 2.60 eV. The optical band gap and the corresponding exciton binding energy are 2.50 and 0.58 eV, respectively, for the in-plane polarized light. The simulated sub-7 nm- L_g DG ML InSe MOSFETs reveal an excellent device performance in the ballistic limit. The n-type ML InSe MOSFETs can satisfy the ITRS 2013 HP and LP standards for the 2028 horizon down to 3 and 5 nm, respectively, whereas the p-type ones can satisfy the HP and LP standards both down to 3 nm. The ML InSe devices are superior to the MoS₂ ones in terms of the larger on-current and superior to the BP ones in terms of the higher stability. Therefore, ML InSe joins the promising channel material candidates to enable Moore's Law down to the sub-5 nm region.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.8b06427.

Many body effect (Section 1); $N_{e/h}$ -dependent transfer characteristics of the DG ML InSe MOSFETs (Section 2); function of UL structures (Section 3); L_g -dependence of intrinsic gate capacitance, quantum capacitance,

transconductance, and field effect mobility of the ML InSe MOSFETs (Section 4); device performance benchmark of the simulated DG ML InSe FETs against the simulated DG ML MoS₂ and BP FETs without UL (Section 5); reliability of the ab initio DFT-NEGFT transport simulation (Section 6) (PDF)

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J.L. conceived the idea. Y.W. and R.F. performed device simulations and electronic calculations. R.Q., J.L., H.Z., X.Z., B.S., and Z.S. took part in the data analyses. Y.W. and R.F. wrote the manuscript. L.X. J.Y., J.S. F.P., and J.L. supervised these investigations. All the authors took part in discussion on results and preparation of the manuscript.

Notes

The authors declare no competing financial interest.

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