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Sub-10 nm two-dimensional transistors: Theory and experiment

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ABSTRACT

Presently Si-based field-effect transistors (FETs) are approaching their physical limit, and further scaling their gate length down to the sub-10 nm region is becoming extremely difficult. Benefitting from the atomic-scale thickness and dangling-bond-free flat surface, two-dimensional semiconductors (2DSCs) have good electrostatics and carrier transportability. The FETs based on the 2DSC channel have the potential to scale the FETs' gate length down to the sub-10 nm region while avoiding apparent degradation of the device performance. In this review, we introduce the recent experimental and *ab initio* quantum transport simulation progress in the 2D FETs with a gate length less than 10 nm. Remarkably, in the extremely optimistic condition, many 2D FETs (*i.e* phosphorene, silicane, arsenene, tellurene, WSe_2, InSe, Bi_2O_2Se, GeSe, *etc.*) show excellent device performance for the high performance and/or low power applications

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Density functional theory

and indeed can extend Moore's law down to 1∼2-nm gate length in terms of the *ab initio* quantum transport simulation. The sub-10 nm 2D tunneling FETs are predicted to generally have smaller energy-delay products compared with the 2D metal–oxide–semiconductor FETs and appear more competitive for the low power application. The carrier effective mass plays a key role in determining the device performance. Via negative capacitance techniques, the device performance can be further improved. Finally, we outline the challenges and outlook on the future development directions in the sub-10 nm 2D FETs.

Contents

1. Introduction

A field-effect transistor (FET) is recognized as one of the most important inventions of the last century. Large scale integrated circuit based on complementary metal–oxide–semiconductor (CMOS) FET is the cornerstone of the information age. The size of the FETs keeps shrinking to increase the FET number on a chip and thus the function of a chip in the past 50 years and follows Moore's law (Fig. 1.1) [1]. Today, a typical chip contains ten billion transistors. To follow Moore's law, not only the circuit integration degree should be increased by scaling, but also the electrical performance of the scaled MOSFETs has to be improved simultaneously. Notably, the energy consumption required within a single switching must exponentially decrease while the transistor switching speed must exponentially increase. Only if the three benefits – smaller, more power-efficient, faster – are accomplished simultaneously, Moore's Law will continue.

The currently dominant Si MOSFET architecture is FinFET, which replaces the previous planar Si MOSFET by significantly improving the gate control. Now the Si FinFETs on the market have the gate length down to about 18 nm. In the 2013 edition of the International Technology Roadmap of Semiconductor (ITRS) [2], the aggressive scaling of the gate length down to 5 nm is required (Fig. 1.1(a)), but further device performance and energy efficiency are tough to improve via simply scaling the gate length. The reason lies in the fact that the short channel effect [3] is dominant in the sub-10 nm scales. Besides, the cost increases rapidly with the reduced MOSFET size and becomes unaffordable. Finally, low power consumption (smart phone, tablet, and laptop) has exceeded high performance and becomes the chief driver of the market. To continue to improve the device performance and continue Moore's law, people make tremendous efforts on updating the device architecture, utilization of alternative information processing principles, or replacing silicon channel with an alternative material [4]. Reducing the pitch can increase the FET density without reducing the size of a single FET (pitch scaling). Nanosheet and nanowire, gate all around (GAA) structure (lateral GAA and vertical GAA), and 3D very large scale integration (VLSI) are believed to be the ultimate device elements in terms of channel geometry, gate electrostatics, and FET density, respectively (Fig. 1.2) [5]. Tunneling FETs (TFETs), negative capacitance FETs (NCFETs), spin FETs, spin-wave devices, and quantum computers work in new principles beyond-CMOS. Alternative channels cover bulk Ge, bulk high-mobility III–V semiconductors, two dimensional (2D) semiconductors (2DSCs) in terms of the International Roadmap for Devices and Systems (IRDS) [6].

In the recent edition (ITRS 2015 version) [7] and its successor, IRDS [6], the scaling of the physical gate length is replaced by the scaling of the technology nodes (Fig. 1.1(b)). The gate length scaling will level off around 12 nm in the 2034 horizon. Although production of the sub-10 nm gate-length MOSFETs is not on the agenda of IRDS at least until 2034, it does not necessarily imply that sub-10 nm gate-length MOSFETs are not useful for future digital CMOS circuits. From the fundamental research point of view, exploring the size limit of a single MOSFET is always the goal to pursue. At the laboratory, many sub-10 nm gate-length FETs have been fabricated, and some exhibit excellent performance. Among them, the 2DSC FETs show great technical potential to work well. In the following, sub-10 nm FET refers to sub-10 nm gate-length FET unless otherwise specified.

First of all, compared with the FETs with bulk semiconductor channels, the FETs with 2D material channels have better gate controllability due to atomic-scale thickness [8–12]. This advantage is relatively straightforward by checking the natural length. We can use a few assumptions to derive the formula for the natural length [13,14], starting from Poisson's equation:

$$\frac{d^2\phi\,(x,y,z)}{dx^2}+\frac{d^2\phi\,(x,y,z)}{dy^2}+\frac{d^2\phi\,(x,y,z)}{dz^2}=\frac{qN_a}{\varepsilon_{ch}} \tag{1.1}$$

where $\phi\,(x,y,z)$ is the scalar electric potential in the channel, q is the unit charge, N_a is the channel doping density, and ε_{ch} is the dielectric constant of the channel (we assume ε_{ch} is a constant). In the case of a wide single-gate Si on insulator (SOI) device, as shown in Fig. 1.3(a), we can simplify Eq. (1.1) by assuming that $\frac{d^2\phi(x,y,z)}{dz^2}=0$:

$$\frac{d^2\phi(x,y)}{dx^2}+\frac{d^2\phi\,(x,y)}{dy^2}=\frac{qN_a}{\varepsilon_{ch}} \tag{1.2}$$

Young [16] assumes a parabolic function in the y-direction:

$$\phi\,(x,y)\approx c_0\,(x)+c_1\,(x)\,y+c_2\,(x)\,y^2 \tag{1.3}$$

Combined with boundary conditions, Eq. (1.2) can be further simplified into a one-dimensional equation:

$$\frac{d^2\psi\,(x)}{dx^2}-\frac{\psi\,(x)}{\lambda^2}=0 \tag{1.4}$$

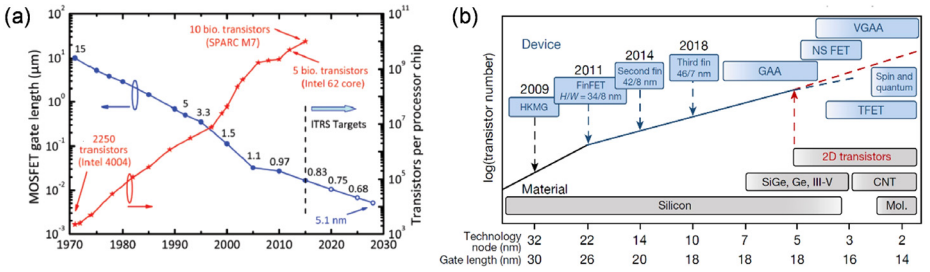


Fig. 1.1. (a) Evolution of the number of MOSFETs integrated on a single microprocessor chip and the gate length of the MOSFETs. The ITRS targets are those for the high-performance logic. (b) Trend of the transistor scaling versus the technology node and physical gate length.
Source: (a) Adapted from Ref. [15]. (b) Reproduced from Ref. [8].

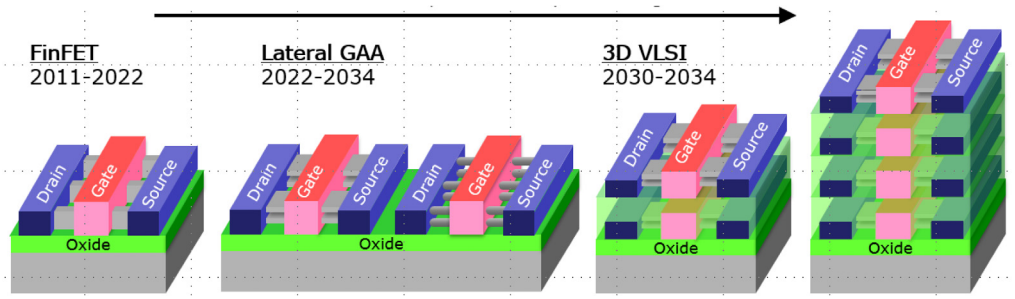


Fig. 1.2. Evolution of FET architecture in terms of IDRS.
Source: Reproduced from Ref. [6].

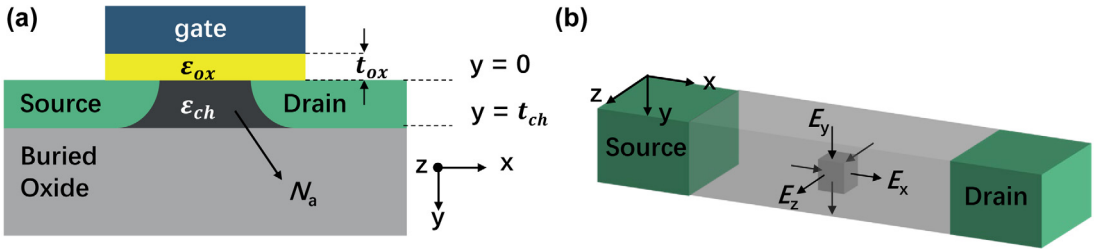


Fig. 1.3. (a) The single-gate silicon on insulator (SOI) device (cross-section). (b) The electrical field along the three directions competes with each other for the controllability of the charge density.
Source: (b) is adapted from Ref. [3].

where

$$\lambda = \sqrt{\frac{t_{ch} t_{ox} \varepsilon_{ch}}{\varepsilon_{ox}}} \tag{1.5}$$

is a characteristic length of a specific device, *i.e.*, the natural length. $\psi(x)$ and $\phi(x, 0)$ differ by a constant. t_{ch} and t_{ox} are the thickness of the channel material and the insulating layer, respectively.

The solution of Eq. (1.4) has an exponential form: $\psi(x) \sim e^{-\frac{x}{\lambda}}$. Thus, we can view λ as the distance across which the electric field can penetrate from the electrode region to the channel region. Similar expressions for natural length can be obtained in multi-gate devices with a geometrical structure correction [3,14]:

$$\lambda = \sqrt{\alpha t_{ch} t_{ox} \frac{\varepsilon_{ch}}{\varepsilon_{ox}}} \tag{1.6}$$

where α is a constant relating to the gate configuration. For the single-gate (SG), double-gate (DG), tri-gate (TG), and gate-all-around (GAA) device structures, α is 1, 1/2, 1/3, and 1/4, respectively.

Generally, we can observe Poisson's equation from another perspective:

$$\frac{d^2\phi(x,y,z)}{dx^2} + \frac{d^2\phi(x,y,z)}{dy^2} + \frac{d^2\phi(x,y,z)}{dz^2} = -\left(\frac{dE_x}{dx} + \frac{dE_y}{dy} + \frac{dE_z}{dz}\right) = \text{a constant value} \tag{1.7}$$

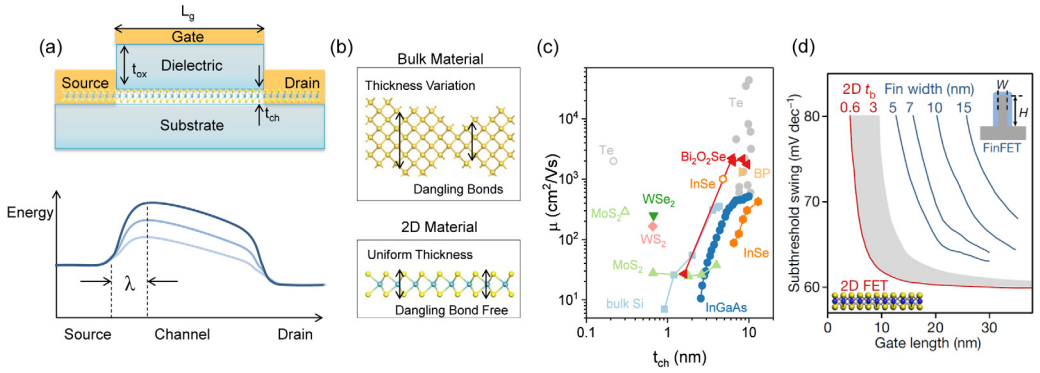


Fig. 1.4. (a) Schematic of a FET and corresponding conduction band profile. λ is the natural length. The conduction band profile is tuned by the gate voltage. L_g is the gate length. t_{ox} and t_{ch} represent the thickness of the gate and channel dielectric, respectively. (b) Comparison of bulk and 2D materials under length scaling. The bulk semiconductor is dominated by thickness variation and rich dangling bonds, while the 2D semiconductor has a uniform thickness and no dangling bond. (c) Thickness-dependent field-effect mobility. When the thickness is decreased to less than 5 nm, the mobilities of 3D bulk semiconductors (e.g. InGaAs [19], Si [11,20–22]) decrease with the bulk thickness ($\mu \propto t^6$). On the other hand, 2D MoS_2 [23–25], Bi_2O_2Se [26], and black phosphorene (BP) [27,28], InSe [29,30], tellurene (Te) [31] have high carrier mobility. Solid and empty symbols stand for data from experiments and calculations, respectively. (d) Subthreshold swing versus the gate length for the transistors with different Fin width or 2D body thickness.
Source: Reproduced from Ref. [11] and Ref. [8].

where E_i is the electric field along the i-direction, as shown in Fig. 1.3(b). In the multi-gate case, the gates control the carrier density through terms $\frac{dE_y}{dy}$ and $\frac{dE_z}{dz}$. The three terms in Poisson's equation add to a constant and compete with each other. Thus, the electric field along the x-direction can reduce the controllability of the gate via the term $\frac{dE_x}{dx}$, which will lead to short channel effects. λ must be less than 1/6 of the channel length to avoid short channel effects [3].

From Eq. (1.6), it is clear that a small natural length can be obtained by reducing the channel thickness t_{ch}. Now the thickness of the ultra-thin-body (UTB) Si semiconductor in FET can reach 6 nm, and the natural length is estimated to be $\lambda = 30.3$ Å by assuming $\alpha = 1$, $t_{ox} = 5$ Å, $\varepsilon_{ox} = 3.9$, and $\varepsilon_{ch} = 11.9$. By contrast, taking monolayer (ML) MoS_2 as an example ($\alpha = 1$, $t_{ch} = 3.01$ Å and $\varepsilon_{ch} = 3.3$), the typical natural length of 2DSC is $\lambda = 3.57$ Å. Hence, the gate electrostatics of 2DSCs is much better than that of the present UTB Si (Fig. 1.4(a)).

Second, although the thickness (t_b) of UTB can be further reduced in a complicated way, the carrier mobility μ decreases dramatically with the thickness to the six power ($\mu \sim t_b^6$), resulting in substantial degradation of the device performance [17,18]. As the thickness of UTB Si is reduced to 1 nm, the carrier mobility is even only a few $cm^2/V{\cdot}s$, much lower than that (300 $cm^2/V{\cdot}s$) in bulk form. The reason lies that the rough surface with dangling bonds of bulk semiconductor always decrease the carrier mobility due to the trap state formed at the interface and the scattering by the thickness fluctuation and roughness [5], and this negative effect is prominent with the reduced thickness because the proportion of the carrier at the surface is increased.

By sharp contrast, the absence of a trap state at the channel-dielectric interface because of the dangling-bond-free surface benefits the transport of the carriers (Fig. 1.4(b, c)) [11,32–35]. Moreover, the atomic-scale smoothness avoids scattering induced by roughness [9]. The measured carrier mobility of ML MoS_2 [23] and WSe_2 [24] with a thickness of 0.4 nm have already exceeded 100 $cm^2/V{\cdot}s$. This value is much higher than that of UTB Si with similar thickness. The measured carrier mobility of a few phosphorene [27] even can reach 1000 $cm^2/V{\cdot}s$. The preferred thickness of 2DSCs to exceed 3D bulk semiconductors in carrier mobility is smaller than 3 nm [8]. Namely, monolayer (ML) and few-layer 2D semiconductors have an advantage in FETs. The excellent gate controllability, absence of trap state, and smooth surface allow a small subthreshold swing (SS) of 2DSD even at the sub-10 nm gate length (Fig. 1.4(d)).

The easy stacking in the vertical direction due to the van der Waals interaction between layers enables the continued increase of the number of transistors per chip with a high density [36]. All these advantages render 2D material promising for the sub-10 nm FETs. IRDS has listed 2D materials as one promising channel material for the next generation transistors [5].

After its birth in 2004, the electronic community used to show high expectations of graphene as the successor to silicon [37]. However, the zero band-gap nature makes graphene transistors fail to achieve an off-state [38]. Notably, the 1D form of graphene — carbon nanotube (CNT) with a specific geometry can have a band-gap and is used as a transistor channel [39]. The first FET based on a 2D material channel with a high current on/off ratio is fabricated in 2011, and the used 2D material channel is ML MoS_2 [40]. Unlike graphene, the sizable band-gap makes MoS_2 FETs attracting enormous attention ever since its fabrication. Later, a group of transition metal dichalcogenides (TMDCs) with a structure similar to MoS_2 has been fabricated and investigated for electronics [24,25,41]. With the development of experimental techniques, other 2D materials including group IV-ene (silicene [42] and stanene [43,44]), group V-ene (phosphorene, arsenene, antimonene, and bisthmuthene) [45], group VI-ene (tellurene) [31], InSe, bismuth oxythilinide (Bi_2O_2Se) [26]

Table 1.1
Comparison in the experimental figures of merit between the Si FETs and the CNT FETs [51].

	Si CMOS	CNT (FET)	CNT (FET)
Gate length (nm)	13.4–16.8	10	5
Gate delay (fs)	220	57	43
EDP (Js/μm)	6.79×10^{-29}	1.88×10^{-30}	6.95×10^{-31}

are discovered successively (group X-ene refers to a 2D material consists of group X element). These 2D materials have distinctive features and show their unique advantages for transistors.

Significant progress has been made towards realizing high-performance 2D material-based sub-10 nm FETs. 2D MoS_2 is the first of 2D semiconductors used to fabricate sub-10 nm FETs [46–49]. The TMDCs based FETs with a gate or channel length less than 10 nm have shown excellent switching performance comparable to those of the state-of-the-art silicon devices, such as a high on/off current ratio of 10^7 and an extremely low subthreshold swing of 65 mV/dec. Besides MoS_2, a 4 nm gate-length 2D $MoTe_2$ FET has also been realized experimentally and exhibits a good switch ability [50]. By using innovative techniques, the realization of the sub-10 nm transistors based on other 2D materials can be anticipated soon.

One-dimensional (1D) carbon nanotube (CNT) has a natural length close to those of 2D materials and also a dangling-free smooth surface. Therefore, they should share a similar device performance. The CNT FETs with a gate length in the range of 5–10 nm have been successfully fabricated by Zhang et al. [51]. They indeed perform much better than the silicon MOSFET at a similar scale in terms of the gate delay time and switch energy measured by energy-delay product (EDP) [51] (Table 1.1). The excellent gate delay time and switch energy (the two key figures of merit of a device performance) observed in the CNT FETs cast a new light on the fabrication of high-performance 2D FETs.

It is highly desirable to predict a 2D FET's performance before the experimental realization in light of the extreme difficulty of such experiments. The direct transfer of the text-book transistor knowledge that focuses on the bulk semiconductor-based long-channel devices is not feasible, and simulations on the new scale (sub-10 nm) and new material (2D) are desired. Many quantum transport simulations have been used in simulating the sub-10 nm 2D material-based transistors. However, most of them are based on the semi-empirical method, where the transition matrix is parameterized, and the corresponding results are thus less reliable. By contrast, parameter-free *ab initio* quantum transport simulation can give accurate results. In this review, we introduce the recent theoretical and experimental progress in 2D material-based FETs in the sub-10 nm regime. We focus on the theoretical results of the *ab initio* quantum transport method because it has no dependence on the empirical parameters and presents more reliable results. We will first describe the basics of a typical FET and the principle of *ab initio* quantum transport simulation in Chapter 2. The current development of the most promising sub-10 nm conventional 2D FETss is presented in Chapter 3 to 8. In Chapter 9 and 10, we introduce sub-10 nm 2D tunneling and negative capacitance FETs, respectively. In Chapter 11, the one dimensional (1D) carbon nanotube FETs are introduced. A summary and outlook are provided in the end.

2. Basics

The operating principle of a typical MOSFET is to control the current magnitude via the variation of the gate voltage. The main drives for scaling the transistors come from increased speed and reduced cost. However, as the channel length continues to scale down, the gate controllability over the current becomes weaker. As a result, some unwanted side effects (*i.e.*, the so-called short channel effects) occur, and the leakage currents arise, which degrade the device performance. In addition to the natural length, a set of figures of merits, including subthreshold swing (SS), transconductance, on-state current (I_{on}), on/off current ratio, delay time, and power dissipation indicator, provide further quantitative information [15].

For CMOS logic, the transistors should respond quickly to the gate voltage change, which sets high demands on the gate electrostatics. Subthreshold swing and transconductance are two main measurements to assess gate controllability (Fig. 2.1). *SS* represents the gate voltage difference that is required for the change of an order of magnitude in current and is calculated by the formula $SS = \frac{dV_g}{d\log(I_{ds})}$, where V_g and I_{ds} are the gate voltage and the source to drain current, respectively. The physical limit of *SS* is 60 mV/dec for standard MOSFET, but even smaller *SS* can be obtained by approaches such as applying new device operation principles. Transconductance is defined as the ratio of the current change to the gate voltage change ($g_t = \frac{dI_{ds}}{dV_g}$). *SS* and g_t are usually extracted from the sub- and super-threshold regions of the transfer characteristics, respectively, and a small *SS* and a large g_t in the transistor are desired on an excellent switching performance.

A high on-state current and a low off-state current (I_{off}) are desired since the former implies a high switching speed while the latter implies a small static power dissipation. Correspondingly, a high on/off current ratio is favored. I_{on} is extracted from the transfer curve via the formula $V_g(\text{on}) = V_{dd} + V_g(\text{off})$, where $V_g(\text{off})$ is the gate voltage corresponding to the off state, V_{dd} is the supply voltage, and $V_{dd} = V_b$ (bias voltage). In the ITRS 2013 edition, the off-state currents for HP and LP applications with 5–10 nm channel lengths are 0.1 μA/μm and 2×10^{-5}–5×10^{-5} μA/μm, respectively, and their on-state currents are 900–1450 and 295–458 μA/μm, respectively. In the ITRS 2015 edition, the off-state currents for the

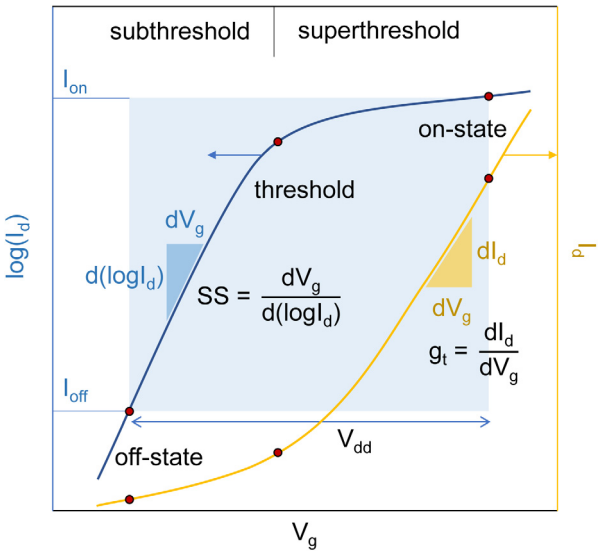


Fig. 2.1. Transfer characteristics of an *n*-type FET. The left axis is logarithmically scaled, and the right axis is linearly scaled. V_g: gate voltage; I_d: source to drain current; *SS*: subthreshold swing; g_t: transconductance; V_{dd}: supply voltage; I_{off}: off-state current; I_{on}: on-state current.

HP logic with 10 nm-gate-length and the LP logic with 12 nm-gate-length are 0.1 and 1×10^{-4} μA/μm, respectively, and the corresponding on-state currents are 1391–1476 and 629–821 μA/μm, respectively, depending on the device structure. In the recent IRDS 2020 edition, the off-state currents for the HP logic with 12 nm-gate-length and the HD (high-density or low-power) logic with 12 nm-gate-length are 1×10^{-2} and 1×10^{-4} μA/μm, respectively, and the corresponding on-state currents are 760–924 and 347–521 μA/μm, respectively.

To directly measure the on/off state switching speed, the delay time is usually used. Effective delay time can be calculated using the formula: $\tau = C_t V_{dd}/I_{on}$, where C_t is the total gate capacitance, and I_{on} the on-state current. C_t is the sum of the fringing capacitance (C_f) and the intrinsic gate capacitance (C_{int}).

$$C_t = C_{int} + C_f \tag{2.1}$$

$$C_{int} = \frac{\partial Q_{ch}}{\partial V_g} \tag{2.2}$$

Q_{ch} is the central region's total charge. The fringing capacitance originates from the fringing fields emitting from the two sides (facing the source and drain) of the gate metal. The intrinsic delay time can be calculated from $\tau_{int} = C_{int}V_{dd}/I_{on}$.

Besides speed, power consumption is a major concern, and power dissipation indicator or power-delay product (PDP) is a good figure of merit, which stands for the energy that an on/off switching needs. The effective PDP can be calculated using the formula: $PDP = V_{dd}I_{on}\tau = C_{total}V_{dd}^2$.

A gated two-probe model is built to simulate a FET. It consists of semi-infinite left electrode, central region, and semi-infinite right electrode, dielectric layer, and metal gate (Fig. 2.2(a)). The accurate theoretical approach to study the electron transport in a FET is the state-of-the-art *ab initio* quantum transport simulation, which is based on nonequilibrium Green's function (NEGF) formalism coupled with density functional theory (DFT) [52].

When a current flows under a finite bias voltage, the FET is in a non-equilibrium state, and the spatial electron density distribution is nonstatic. DFT is originally established for static electron density. The Kohn–Sham formulation of DFT is expressed as [55]:

$$\left(-\frac{\hbar^2}{2m}\nabla^2 + V_{eff}(n)\right)\varphi_i(r) = \varepsilon_i\varphi_i(r)$$

$$V_{eff}[n] = V_H[n] + V_{xc}[n] + V_{ext}[n] \tag{2.3}$$

where $V_H[n]$ is the Hartree potential describing the classical electrostatic interaction between the electrons. $V_{xc}[n]$ is the exchange–correlation energy. $V_{ext}[n]$ is the sum of the electrostatic potential energy of the electrons in the ions potential and other electrostatic field sources, for example, the gate voltage V_{gate}. The total external potential is given by

$$V_{ext} = \sum_a V_{pseudo}^a + V_{gate} \tag{2.4}$$

where V_{pseudo}^a includes the local (V_{loc}^a) and nonlocal (V_{nl}^a) pseudopotential contributed by the *a*th atom.

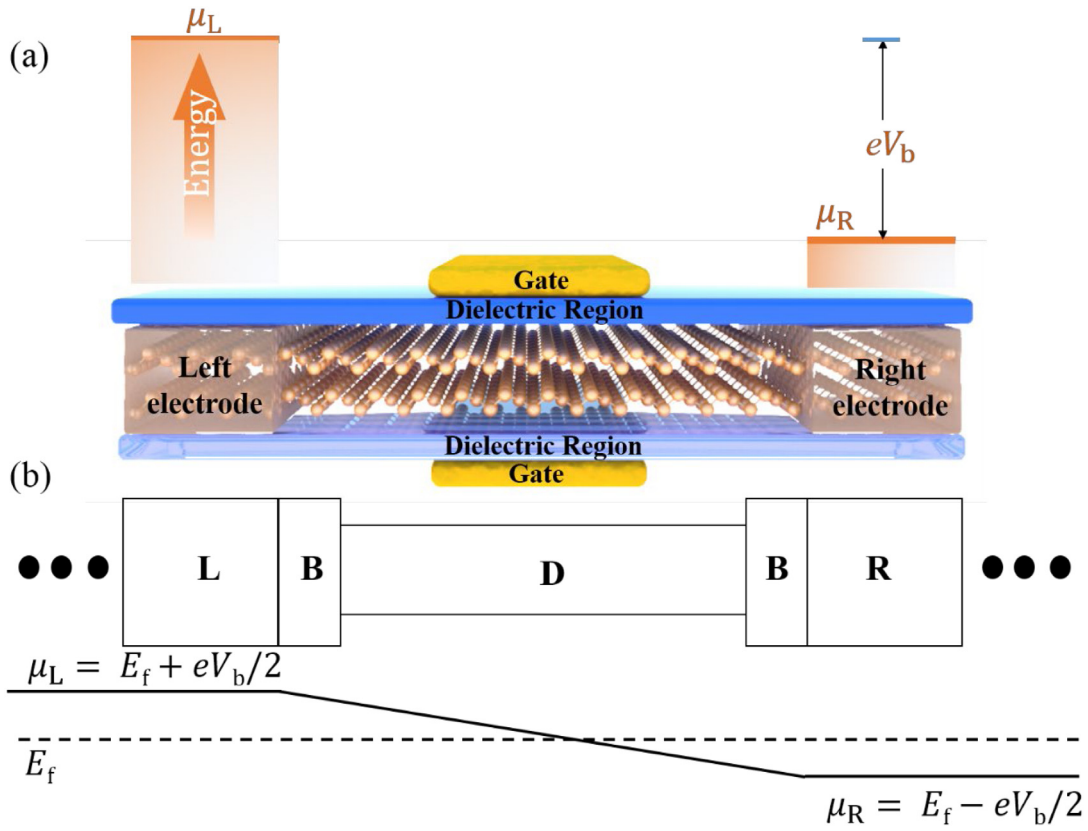


Fig. 2.2. (a) A typical gated two-probe model device system. (b) Potential drop through a FET due to a bias voltage. L, R, B, D represent the left electrode, right electrode, buffer region, and device (channel) region, respectively. μ_L and μ_R are the electrochemical potentials of the left and right electrodes, respectively. E_f is the Fermi level. V_b is the voltage of bias.
Source: (a) Reproduced from Ref. [53]. (b) Reproduced from Ref. [54].

We assume the electron transport in the FET remains in a steady-state, and thus electron distribution can still be described by static DFT. The bias leads to a split of the chemical potential of the left and right electrodes, and the electrode electrostatic potentials set up the boundary conditions for the central region electrostatic potential. The correction of the V_{eff} caused by extra electron density is carried out by using the Poisson equation: $\nabla^2 V_{\text{eff}}(\boldsymbol{r}) = -4\pi\rho_{\text{extra}}(\boldsymbol{r})$. We have $\rho_{\text{extra}}(\boldsymbol{r}) = \rho_{\text{neq}}(\boldsymbol{r}) - \rho_{\text{eq}}(\boldsymbol{r})$, where $\rho_{\text{neq}}(\boldsymbol{r})$ is the electron density in the nonequilibrium state, and $\rho_{\text{eq}}(\boldsymbol{r})$ is the electron density in the equilibrium state. Fig. 2.2 stands for the natural boundary condition of the Poisson equation. The potential drop solely arises in the device part and is a constant in the electrode region because of strong screening. The periodic and Neumann conditions are used on the electrode boundaries along the transverse direction and the direction orthogonal to the 2D semiconductor surface, respectively.

The density can be split into three parts, the extended electronic states from the left and right electrodes and bound states in the central region.

$$n(\boldsymbol{r}) = n_L(\boldsymbol{r}) + n_R(\boldsymbol{r}) + n_B(\boldsymbol{r}) \tag{2.5}$$

According to the scattering theory, the extended electronic states from the left and right electrodes can be obtained by summing up the occupied scattering states,

$$n_L(r) = \sum_\alpha \left|\psi_\alpha^L(r)\right|^2 f\left(\frac{\varepsilon_\alpha - \mu_L}{k_B T_L}\right) \tag{2.6}$$

$$n_R(r) = \sum_\alpha \left|\psi_\alpha^R(r)\right|^2 f\left(\frac{\varepsilon_\alpha - \mu_R}{k_B T_R}\right) \tag{2.7}$$

where ψ_α^L and ψ_α^R is the scattering state from the left and right electrode, respectively, and $f(x) = (1 + e^x)^{-1}$ is the Fermi–Dirac distribution.

Non-equilibrium Green's function (NEGF) formalism is formally equivalent to the scattering state method and gives identical results. The density matrix in the nonequilibrium state of the NEGF formalism consists of the left and right

contributions,

$$D = D^{\mathrm{L}} + D^{\mathrm{R}} \tag{2.8}$$

The left contribution is calculated as [56]

$$D^{\mathrm{L}} = \int A^{\mathrm{L}}(\varepsilon) f(\frac{\varepsilon - \mu_{\mathrm{L}}}{k_{\mathrm{B}} T_{\mathrm{L}}}) d\varepsilon \tag{2.9}$$

where

$$A^{\mathrm{L}}(\varepsilon) \equiv \frac{1}{2\pi} G(\varepsilon) \Gamma^{\mathrm{L}}(\varepsilon) G^{\dagger}(\varepsilon) \tag{2.10}$$

is the spectral density matrix, expressed in terms of the retarded Green's function G and the broadening function Γ^{L} of the left electrode,

$$\Gamma^{\mathrm{L}} = \frac{1}{i} \left(\sum\nolimits^{\mathrm{L}} - \left(\sum\nolimits^{\mathrm{L}} \right)^{\dagger} \right) \tag{2.11}$$

which is given by the left electrode self-energy $\sum^{\mathrm{L}}$. Besides, the Fermi–Dirac distribution f in the left electrode has an electron temperature T_{L}.

The retarded Green's function matrix for the central region $G(\varepsilon)$ is crucial to NEGF. It is calculated from the central-region Hamiltonian matrix H and overlap matrix S by adding the electrode self-energies,

$$G(\varepsilon) = [(\varepsilon + i\delta_{+}) S - H - \sum\nolimits^{\mathrm{L}}(\varepsilon) - \sum\nolimits^{\mathrm{R}}(\varepsilon)]^{-1} \tag{2.12}$$

where δ_{+} is an infinitesimal positive number. The self-energies describe the effect of the electrode states on the central region electronic structure and are calculated from the electrode Hamiltonians.

The electron density matrix can also be divided into an equilibrium part and a non-equilibrium part. We have

$$D = D^{\mathrm{L}}_{\mathrm{eq}} + \Delta^{\mathrm{R}}_{\mathrm{neq}} \tag{2.13}$$

where

$$D^{\mathrm{L}}_{\mathrm{eq}} = \int d\varepsilon (A^{\mathrm{L}}(\varepsilon) + A^{\mathrm{R}}(\varepsilon)) f(\frac{\varepsilon - \mu_{\mathrm{L}}}{k_{\mathrm{B}} T_{\mathrm{L}}}) \tag{2.14}$$

$$\Delta^{\mathrm{R}}_{\mathrm{neq}} = \int d\varepsilon A^{\mathrm{R}}(\varepsilon) \left[f\left(\frac{\varepsilon - \mu_{\mathrm{R}}}{k_{\mathrm{B}} T_{\mathrm{R}}} \right) - f\left(\frac{\varepsilon - \mu_{\mathrm{L}}}{k_{\mathrm{B}} T_{\mathrm{L}}} \right) \right] \tag{2.15}$$

Equivalently, we could write the density matrix as

$$D = D^{\mathrm{R}}_{\mathrm{eq}} + \Delta^{\mathrm{L}}_{\mathrm{neq}} \tag{2.16}$$

where L and R are exchanged in (2.13) and (2.16). Due to the finite accuracy of the numerical integration, a double contour [56] is always used to get a more accurate result.

When the non-equilibrium density matrix under the given boundary conditions is obtained self consistently, various transport properties of the system can be obtained. The most notable one is the transmission spectrum, which is used to get the current and differential conductance. The transmission coefficient T at a certain electron energy ε is obtained from the retarded Green's function [57],

$$T(\varepsilon) = \mathrm{Tr}[G(\varepsilon) \Gamma^{\mathrm{L}}(\varepsilon) G^{\dagger}(\varepsilon) \Gamma^{\mathrm{R}}(\varepsilon)] \tag{2.17}$$

and the electrical current is given by the Landauer formula [58],

$$I = \frac{2e}{h} \int_{-\infty}^{\infty} d\varepsilon T(\varepsilon) [f\left(\frac{\varepsilon - \mu_{\mathrm{L}}}{k_{\mathrm{B}} T_{\mathrm{L}}} \right) - f\left(\frac{\varepsilon - \mu_{\mathrm{R}}}{k_{\mathrm{B}} T_{\mathrm{R}}} \right)] \tag{2.18}$$

The generalized gradient approximation (GGA) to exchange–correlation functional is widely used in the FET *ab initio* quantum transport simulation. GGA is based on a single-electron approximation and is well known to significantly underestimate the band-gap of the intrinsic semiconductors [59], and the quasiparticle approach (GW method), which takes many-body effects into account, can well reproduce the observed band-gap of the semiconductor. Fortunately, GGA works satisfactorily in the FET simulations due to the band-gap renormalization for two reasons. Firstly, the transistors work with the doped semiconducting channel, in which the abundant electrons in the channel strongly screen the electron–electron interaction [60–62]. For example, the band-gap of the heavily doped ML $MoSe_2$ at the GGA level is 1.53 eV, which is consistent with the renormalized band-gap of 1.59 eV obtained by the GW method and the experimental result of 1.58 eV [63]. Secondly, in a device environment, the dielectric region also strongly screens the electron–electron interaction in the channel. For example, in terms of the GW calculation, the quasi-particle band-gap of free-standing ML MoS_2 is 2.8 eV but normalized to 1.9 eV in a device environment [64], which is close to the band-gap of 1.7 eV at the GGA level [65]. Based on these two reasons, the single-particle approximation adopted by GGA becomes a good

approximation and renders GGA suitable to describe the FET behavior. For example, the transport gaps of ML, BL, and TL black phosphorene FETs with Ni electrode from the simulation at the GGA level are 0.79, 0.81, and 0.68 eV, respectively, which are comparable with the experimental transport gap 0.99, 0.71, and 0.61 eV, respectively [66–69].

Ballistic transport is often adopted in the sub-10 nm FET simulation because the ballistic transport is dominant over the dissipative one when the channel length is less than 10 nm [70,71]. A benchmark is made to prove the reliability of the *ab initio* quantum transport simulation at the GGA level for the sub-10 nm FETs by comparing the performance of the simulated 2D MoS_2 and 1D CNT transistors with the respective experimental ones. A general agreement is found in the overall transfer characteristics in the 1 nm-gate-length 2D MoS_2 transistors with extremely thin effective oxide thicknesses [49,72]. The simulated *SS* of 66 mV dec^{-1} is almost identical to the observed one (65 mV dec^{-1}) [49,72]. The drive currents of the 5–9 nm channel-length ML MoS_2 *n*-type MOSFET are predicted to be 270–290 $\mu A\ \mu m^{-1}$ in the ballistic transport limit at a bias of $V_b = 0.64$ V [73]. These values are close to the drive current 180 $\mu A\ \mu m^{-1}$ at $V_b = 1$ V in the fabricated 10 nm-channel-lengths ML MoS_2 FET with the nearly Ohmic graphene-MoS_2 contact [46]. The calculated transfer characteristics, on-state current, delay time, and power dissipation of the 5 nm-gate-length CNT FET are even in better agreement with the observed ones (Section 11).

3. Sub-10 nm 2D TMDC FETs

3.1. Fundamental properties of 2D TMDC

Transition metal dichalcogenides (TMDC) are layered crystals noted as MX_2 (M = Mo or W, and X = S, Se, or Te). Each layer of the crystal consists of three planes (X-M-X planes) and each of the planes is covalently bonded. Structures of bulk MX_2 can be distinguished by different stacking orders of the X-M-X planes, *i. e.* ABA for 2H phase (hexagonal symmetry) and ABC for 1T phase (tetragonal symmetry) (Fig. 3.1(a)) [74–77]. The dimerization of the transition metal atom in the 1T phase results in the 1T′ phase. The 2H phase of MX_2 is semiconducting with band-gaps of the order of eV, while 1T and 1T′ phases are metallic [76,78]. Unless otherwise specified, the MX_2 materials discussed below are all in their 2H semiconducting phases.

DFT calculation shows that the band-gap of MX_2 increases while the number of layers decreases (Fig. 3.1(b)). The band-gaps of bulk MX_2 are indirect and range from 1.0 to 1.4 eV, and the band-gaps of ML MX_2 are direct and range from 1.2 to 2.1 eV [79]. GW correction usually enlarges DFT band-gaps by about 50% while keeping band-gap-centers almost unmoved [80,81]. The bandgaps of ML MoS_2 and ML WS_2 extracted from the scanning tunneling spectroscopy (STS) experiments are 2.16 ± 0.04 eV and 2.38 ± 0.06 eV, respectively [82].

The research of thin MoS_2 flakes can date back to 1963 [83], and the first ML MoS_2 was obtained in 1986 [84]. The techniques developed for graphene are well-suited for layered MX_2, which stimulated the renaissance in this field. Current ML and few-layer (FL) MX_2 fabrication approaches include mechanical exfoliation, liquid-phase exfoliation, chemical vapor deposition (CVD), and molecular beam epitaxy (MBE) [74]. A wafer-scale highly-oriented ML MoS_2 has been grown via the CVD method, exhibiting moderate mobility of around 40 $cm^2/V{\cdot}s$ [85].

The first-principles calculation suggests that the intrinsic phonon-limited mobility of ML MoS_2 at room-temperature ranges from several tens to a few thousands of $cm^2/V{\cdot}s$, and low-temperature mobility exceeds 10^5 $cm^2/V{\cdot}s$, depending on the internal and external conditions, such as impurity density and dielectric environment [70,86,87]. The transport experiments demonstrated that the mobility of an ML MoS_2 transistor could reach about 200 $cm^2/V{\cdot}s$ at room temperature [40] and 1020 $cm^2/V{\cdot}s$ at low temperature [88]. Recently, Kim Philip et al. reported unprecedentedly high hole mobility of 30,000 $cm^2/V{\cdot}s$ for ML WSe_2 encapsulated by hexagonal boron nitride [89].

3.2. Experimental sub-10 nm 2D TMDC FETs

In 2011, Kis's group fabricated the first ML MoS_2 transistor. The channel length of this transistor is 1.5 μm. It shows a current on/off ratio as high as 10^8 and a low *SS* of 74 mV/dec at a bias voltage of 0.5 V [40]. These results demonstrated the superior properties of 2D MoS_2. Although exposure to ambient may reduce the performance of 2D MoS_2 transistors, the absorbates can be efficiently removed by vacuum annealing, and then the device performance will recover [90].

The first sub-10 nm 2D MoS_2 transistor came out in 2016, in which a single-walled carbon nanotube (SWCNT) with a diameter of 1 nm serves as the gate (Fig. 3.2(a)) [49]. This 1 nm-gate-length bilayer (BL) MoS_2 device showed an extremely low *SS* of 65 mV/dec and a large current on/off ratio of 10^6 at a bias voltage of 1 V, demonstrating suppression of short channel effect. By using the linear extrapolation method, we can estimate the on-state current of this BL MoS_2 FET with a gate length of 1 nm to be only 1 μA/μm at a supply voltage of 0.64 V. The low on-state current may result from the relatively long channel length (hundreds of nanometers) and the sizeable Schottky barrier of bulk Ni electrical contact (about 150 meV) [91] that leads to a significant scattering to electrons.

It is very easy to form defects and impurities at the electrode–channel interface when using conventional step-by-step processes, and the composited interface forms a Schottky barrier and results in poor performance of the devices [50]. A systematical work based on first-principle quantum transport simulations shows that in the ML MX_2 FETs with 2H-1T′ electrodes, the Schottky barrier height becomes tunable by the gate voltage, leading to a more effective carrier transmission and a lower contact resistance [65].

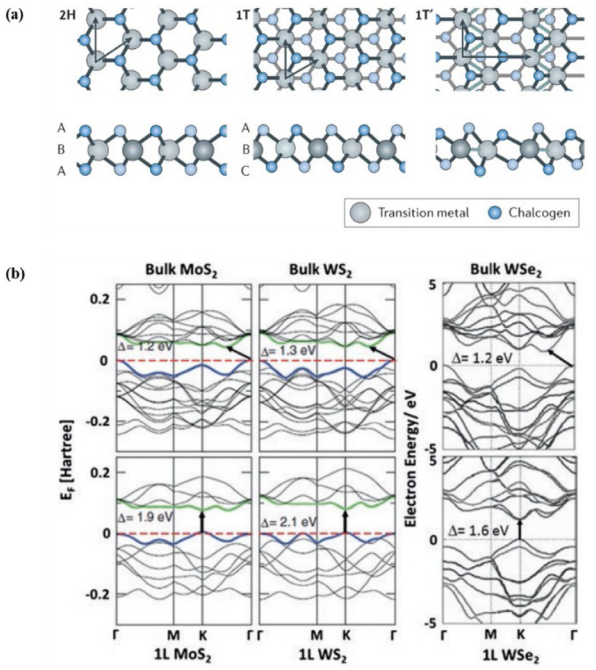


Fig. 3.1. (a) Schematic of 2H, 1T, and 1T′ structures of MX_2 [74]. (b) Energy band structures of bulk and ML MX_2 based on DFT calculation [79]. *Source:* (a) is adapted from Ref. [74]. (b) is adapted from Ref. [79].

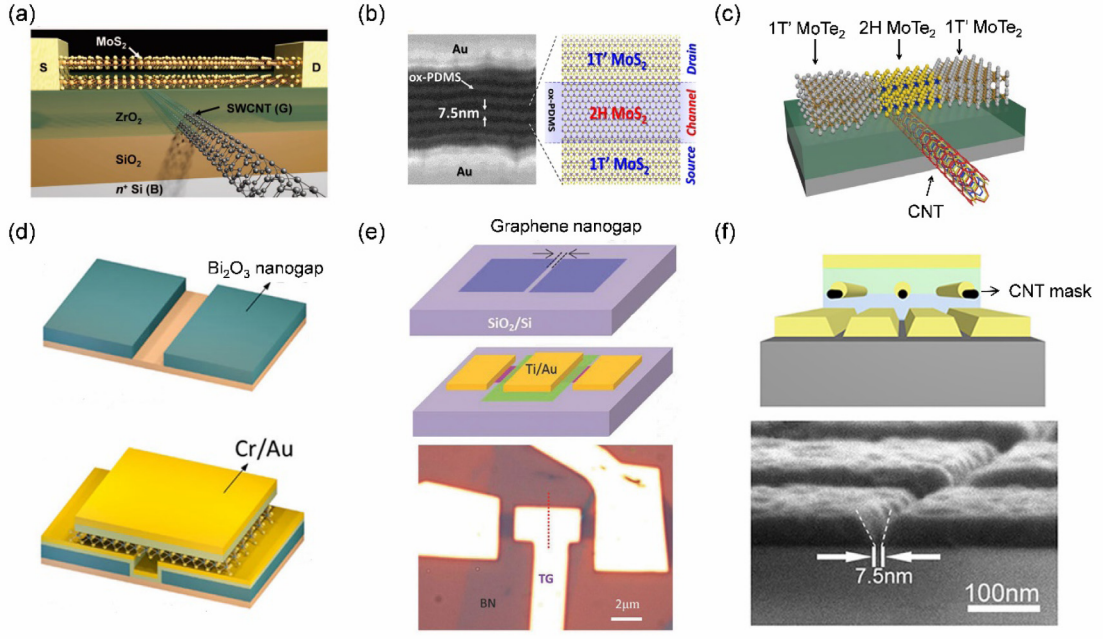


Fig. 3.2. Sub-10 nm MX_2 transistors. (a) Schematic of the 1D/2D-FET with an SWCNT gate and a BL MoS_2 channel. (b) SEM and schematic images of the 1T′-2H contact MoS_2 FETs with a 7.5 nm channel length. (c) Schematic image of the CNT-gated 2D 1T′-2H $MoTe_2$ FET. (d) Schematic images of an 8.2 nm channel length ML MoS_2 FET fabricated by making use of the Bi_2O_3 nanogaps. (e) Schematic and optical microscope images of graphene-contacted 3.8 nm channel length top-gated MoS_2 devices. (f) Schematic and SEM image of a 7.5 nm channel length ML MoS_2 FET using CNT as an evaporating mask.
Source: (a) Adapted from Ref. [49]. (b) Adapted from Ref. [47]. (c) Reproduced from Ref. [50]. (d) Reproduced from Ref. [48]. (e) Adapted from Ref. [46]. (f) Adapted from Ref. [92].

Table 3.1
Key parameters of the fabricated sub-10 nm 2D MX_2 transistors.

Channel	L_g (nm)	L_{ch} (nm)	I_{on} (μA/μm)	I_{on}/I_{off}	*SS* (mV/dec)	V_b (V)	
BL MoS_2	1	∼560		10^6	65	1	CNT gate [49]
TL MoS_2		7.5	250	10^7	120	1	1T′ phase electrodesix FETs in-series [47]
ML MoS_2		8.2	1	10^6	140	1	Bi_2O_3 nanogap [48]
ML MoS_2		3.8	10		208	0.1	Graphene nanogap [46]
ML MoS_2		7.5	45	10^7	120	1	CNT mask [92]
ML $MoTe_2$	4		5	10^5	73	0.88	1T′ phase electrodeCNT gate [50]

L_g: gate length, L_{ch}: channel length, I_{on}: on-state current, I_{on}/I_{off}: on/off current ratio, *SS*: subthreshold swing, and V_b: bias voltage.

To reduce the contact resistance and simplify the fabrication process, Tomás Palacios et al. employed directed self-assembly of the block copolymer as a mask to fabricate 7.5 nm-channel-length ML and trilayer (TL) MoS_2 transistors with metallic 1T′ phase as electrode [47] (Fig. 3.2(b)). The resulting device is comprised of a chain of six 7.5 nm-channel-length 2D MoS_2 FETs in-series. The chain of in-series MoS_2 FETs shows a low off-state current of 10 pA/μm and a large on-state current of 250 μA/μm, resulting in a high current on/off ratio of 10^7 at a bias voltage of 1 V.

Besides MoS_2, one can employ the 1T′-2H interface engineering in other types of TMDCs, such as $MoTe_2$ [77,93]. Various chemical vapor techniques are used to synthesize the $MoTe_2$ 2H-1T′ interface [87,94]. Based on the hetero-phase interface techniques of 2D $MoTe_2$, a FET with 2H-$MoTe_2$ channel and 1T′-$MoTe_2$ electrodes is fabricated using a 4 nm-diameter-CNT as the gate (Fig. 3.2(c)). HfO_2 with a high dielectric constant serves as the dielectric layer, and 1T′-2H 2D $MoTe_2$ is subsequently synthesized on the HfO_2 dielectrics. The 4 nm-gate-length FET demonstrates excellent switching characteristics with a high on/off current ratio of 10^5, a small maximum current of 5 μA/μm at a bias voltage of 0.88 V, and a small *SS* of 73 mV/dec [50].

Jun He et al. used corrosion crack along the cleavage plane of Bi_2O_3 to fabricate a single ML MoS_2 FET with an 8.2 nm channel length [48] (Fig. 3.2(d)). The resulting current on/off ratio and *SS* are 10^6 and 140 mV/dec, respectively. However, the maximum current is less than 1 μA/μm at a bias voltage of 1 V. Utilizing the graphene nanogaps (Fig. 3.2(e)), Zhang's group successfully fabricated the ML MoS_2 FETs with 4 nm-channel-length [46]. The maximum current is 10 μA/μm, and the *SS* is relatively high (208 mV/dec) at a supply voltage of 100 mV. While the Bi_2O_3 thin-film nanogaps and graphene nanogaps form randomly and lead to a low yield, the application of SWCNT film as an evaporation mask allows for large-scale fabrication of sub-10 nm MoS_2 FETs [92] (Fig. 3.2(f)). The fabricated 7.5 nm-channel-length ML MoS_2 transistor exhibited excellent performances with an on/off ratio up to 10^7 and a *SS* of about 120 mV/dec.

The critical parameters of the fabricated sub-10 nm 2D MX_2 transistors are summarized in Table 3.1. *SS* shows a clear relation with the channel length. The devices with the lowest *SS* (65 and 73 mV/dec) possess the longest channel length of about hundreds of nanometers, while the one with the largest *SS* (208 mV/dec) possesses the shortest channel length. The direct source to drain tunneling leakage plays a significant role in the gate controllability in these cases. The on-state current ranges on a large scale, even for those with similar gate lengths of about 7 nm. The one with the 1T′ MoS_2 electrodes shows a remarkable on-state current of 250 μA/μm thanks to the channel's low defect density and the optimized electrical contact [47].

3.3. Experimental 2D MoS_2 CPU

Though 2D materials like FL TMDCs have been considered promising candidates for constructing next-generation HP and LP integrated circuits (ICs), the growth of large-area uniform 2D materials has been an obstacle and hinders their practical applications. Kah-Wee Ang et al. have succeeded in synthesizing wafer-scale ML MoS_2 by the CVD method [92]. They also successfully demonstrated transistors, memristive memories, and small ICs such as Boolean logic circuits based on the synthesized material. Based on CVD-grown large-area BL MoS_2 uniform films, Thomas Mueller et al. presented a 1 bit microprocessor unit (CPU) consisting of 115 transistors [95]. The CPU includes a control unit (CU), an instruction register (IR), a program counter (PC), an accumulator (AC), an output register (OR), and an arithmetic logic unit (ALU) with inputs A and B as shown in Fig. 3.3. With these essential components, this 1 bit CPU can execute programs stored in an external memory module and basic logical operations, such as conjunctions and disjunctions at a frequency of up to 50 Hz. Although the demonstration is only 1 bit, it is possible to extend it to multi-bit computation. This is the most complex large-scale integrated circuits demonstration made of 2D materials, which opens up more possibilities for further large-scale circuits implementations.

3.4. Simulation of sub-10 nm ML TMDC FETs

The FET with metal electrodes is termed as Schottky barrier FET (SBFET) (Fig. 3.4(a)) and that with the degenerately doped 2D semiconductor as electrodes termed as MOSFET (Fig. 3.4(c)). The former's performance is usually poorer due to the pervasive existence of the Schottky barrier between the electrode and channel. However, the experimental transistors based on the 2D semiconductor are usually SBFETs because a proper doping method lacks [35], and metal is often used as

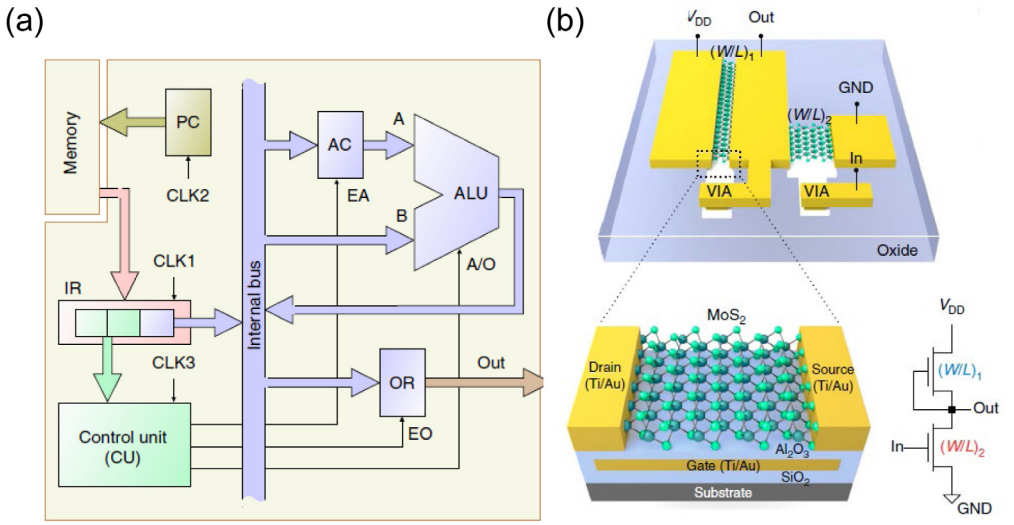


Fig. 3.3. (a) Components of the 1 bit microprocessor: a PC, an IR, a CU, an AC, an OR, and an ALU with inputs A and B. CU supplies enable signals (EA and EO) and operation selection code (A/O) to the respective subunits. Clock (CLK)-signal generation and memory components are off-chip. (b) Schematic of an inverter made of a 2D MoS_2 transistor (bottom panel) and the corresponding circuit architecture.
Source: Adapted from Ref. [95].

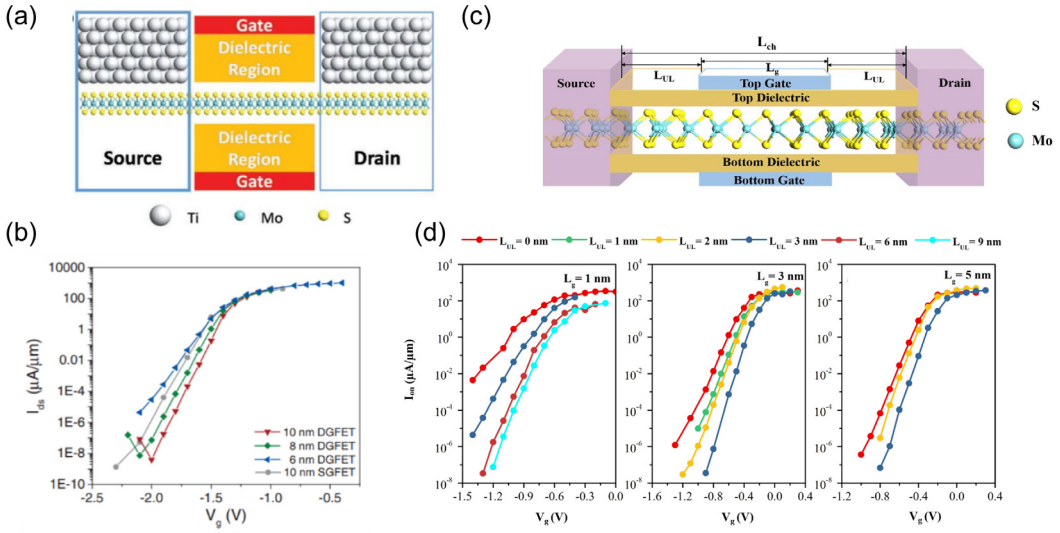


Fig. 3.4. (a) Schematic of an ML MoS_2 DG SBFET with a metal electrode. (b) Transfer characteristics of MoS_2 DG SBFETs with channel length L_{ch} = 6, 8, and 10 nm and MoS_2 single gated (SG) FET with L_{ch} = 10 nm. The bias voltage V_{ds} is set to be 0.5 V. (c) Schematic of an ML MoS_2 DG MOSFET. (d) Transfer characteristics for the n-type ML MoS_2 MOSFETS with L_g = 1, 3, and 5 nm and different L_{UL}, respectively. These transfer characteristics are from the *ab initio* quantum transport simulation.
Source: (a, b) Adapted from Ref. [96]. (c, d) Adapted from Ref. [97].

an electrode. When metal is used as an electrode, the Schottky barrier is often formed at the metal–channel interface due to the Fermi level pinning [12]. The semi-empirical quantum transport simulations based on the NEGF formalism show that BL MoS_2 MOSFETs can meet the ITRS 2013 edition HP on-state current requirement up to L_g = 6.6 nm, while the LP on-state current requirement cannot be met for ML, BL, and TL MoS_2at all the sub-10 nm gate lengths [98]. Since ITRS 2013 edition generally is related to the sub-10 nm gate length and has a stricter standard than the latter version, and in the following, ITRS standard means ITRS 2013 version standard unless otherwise mentioned.

The calculated transfer characteristics of the sub-10 nm DG ML MoS_2 SBFETs and MOSFETs from the *ab initio* quantum transport simulation are shown in Fig. 3.4(b) and (d), respectively (the label DG is omitted unless otherwise specified). Underlap (UL) structure is the uncovered part of the channel by the gate electrode (Fig. 3.4(c)) and is often used to improve the device performance. On the one hand, it increases the source-to-drain barrier length, and thus the source-to-drain

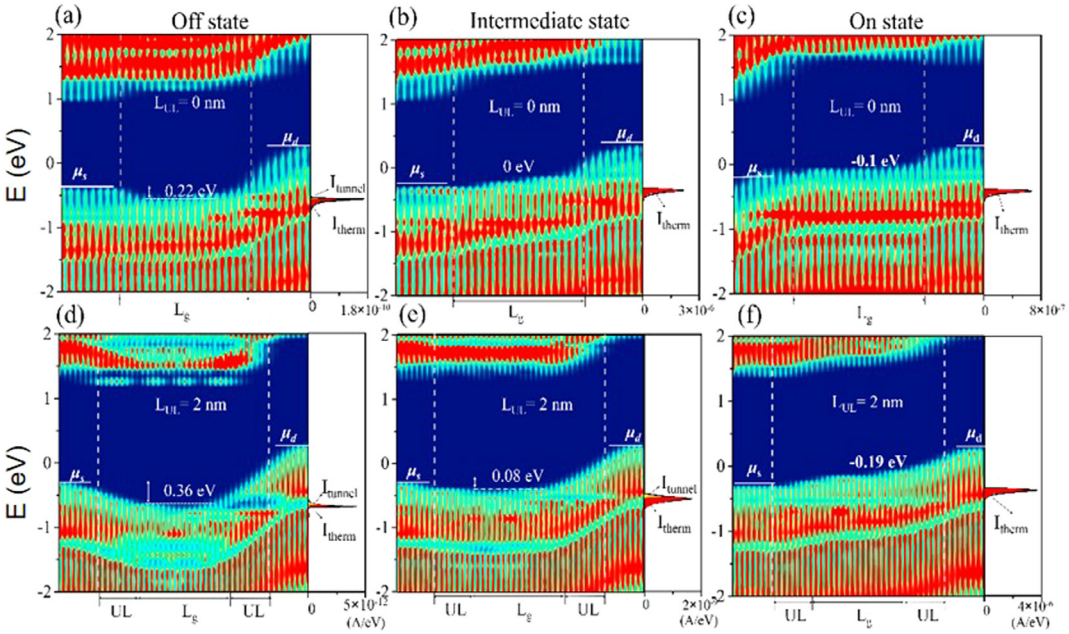


Fig. 3.5. (a–f) Local device density of states (LDDOS) and spectral current of the 5 nm-L_g *p*-type DG ML MoS_2 MOSFETs with $L_{UL} = 0$ and 2 nm at the off, intermediate, and on states for the LP applications, respectively. μ_s (μ_d): electrochemical potential of the source (drain). Φ_{max}: maximum hole barrier height.
Source: Reproduced from Ref. [97].

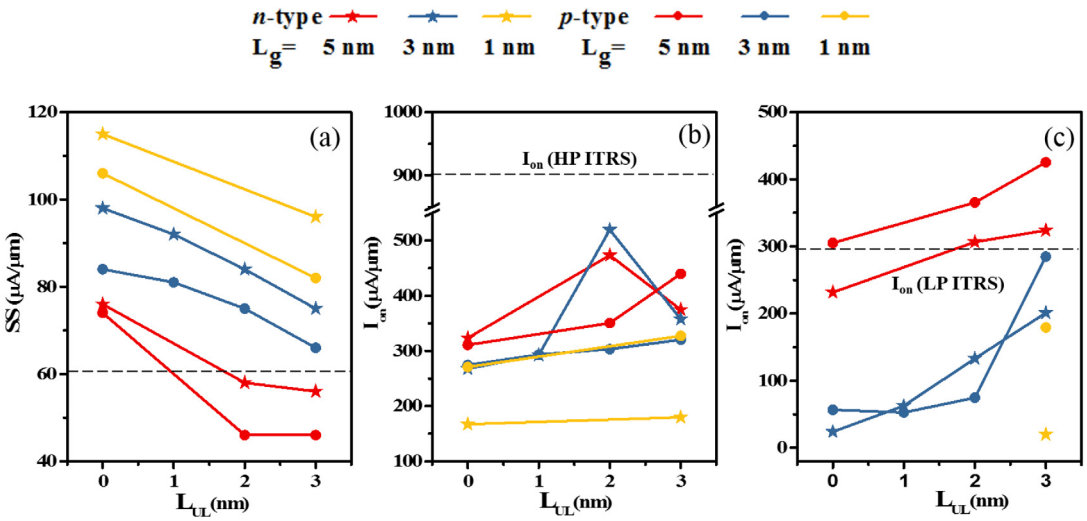


Fig. 3.6. (a) *SS*, (b) HP-I_{on}, and (c) LP-I_{on}versus L_{UL} for the *n*- and *p*-type DG ML MoS_2 DGFETs. The black dashed line in (a) indicates the Boltzmann limit of 60 mV/dec for *SS* at room temperature and in (b)/(c) represents the ITRS HP/LP requirements.
Source: Reproduced from Ref. [97].

leakage is suppressed in favor of device performance. On the other hand, the gate control to the uncovered channel is not as strong as the covered part. Besides, the UL structure increases the scattering probability of electrons. When introducing a 2 nm UL structure, the maximum barrier height Φ_{max} (namely, activation energy) at the off-state of the DG ML MoS_2 *p*-MOSFETs with $L_g = 5$ nm is increased from 0.22 to 0.36 eV. The spectral current peak also increases significantly at the on-state (Fig. 3.5). As shown in Fig. 3.6, the longer UL structures, the smaller *SS* of DG ML MoS_2 MOSFETs. However, the on-state current does not completely monotonically rise with the increase of UL structure. Therefore, the UL length should be optimized.

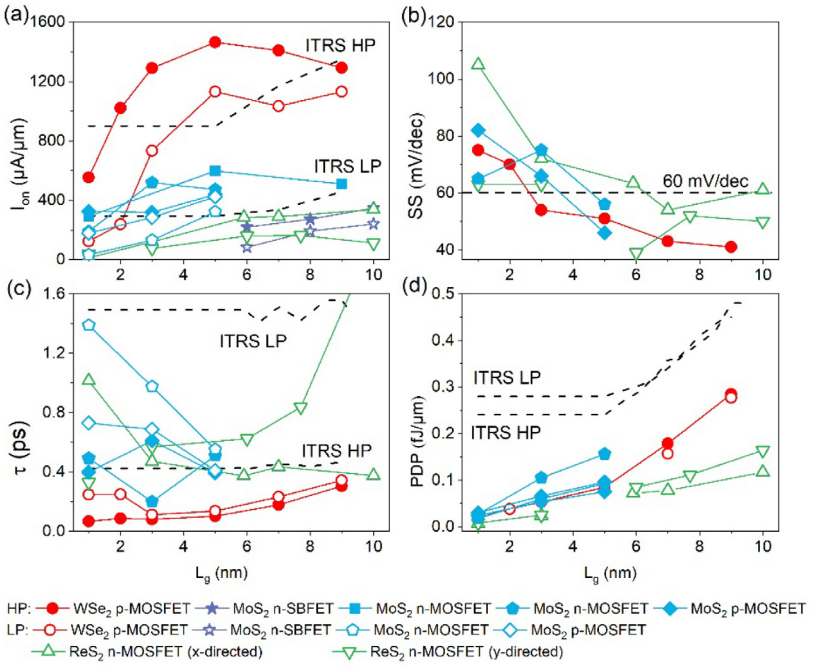


Fig. 3.7. Calculated figures of merit of the ML MX_2 FETs as a function of the gate length. These data are from the first-principle simulations with consideration of UL. (a) On-state current, (b) subthreshold swing, (c) intrinsic delay time, and (d) PDP. The solid and open symbols stand for the results calculated with the ITRS HP and LP parameters, respectively. The data are from Refs. [96,99–101].

The calculated on-state currents of the ML MoS_2 MOSFETs and SBFETs from the first principles quantum transport simulations are compared in Fig. 3.7(a). The former shows a higher on-state current than the latter due to the barrier-free contact and adoption of a UL structure. With a proper UL, the ML MoS_2 MOSFETs show on-state currents approaching the ITRS LP goals [7] and delay time and PDP meeting the LP goals at $L_g = 5$ nm. However, the on-state currents of the sub-10 nm MoS_2 MOSFETs fail to meet the ITRS goals for the HP applications, and the delay time is also larger than the corresponding ITRS goals in most cases [97].

ML WSe_2 and MoS_2 share similar hexagonal crystalline structures and band-gap sizes [102]. However, WSe_2 is more stable than MoS_2 in resisting oxidation when exposed to a humid environment [103,104]. The fabricated ML *p*-type WSe_2 transistor demonstrates a FET mobility of 250 $cm^2/V{\cdot}s$ for holes, *SS* of 60 mV/dec, and on/off ratio of 10^6 at room temperature [24]. With the resort of UL, the corresponding ML DG WSe_2 MOSFETs can satisfy the ITRS HP/LP requirements even when L_g decreases to 2/3 nm (Fig. 3.7(a)) [99]. Most noticeably, the 5 nm-L_g *p*-type ML WSe_2 MOSFET with UL of 1 nm shows a high on-state current of 1132 μA/μm for the LP applications. All the delay time and PDP of the *p*-type ML WSe_2 MOSFETs in different gate lengths under 10 nm can meet and even exceed the criteria of ITRS HP and LP devices for the 2022–2028 horizon [99]. The much better device performance of the ML WSe_2 MOSFETs is mainly ascribed to the fact that ML WSe_2 owns a slightly smaller effective mass (0.46 m_0, m_0 is the free-electron mass) compared with that of the ML MoS_2(0.64 m_0) [105].

ReS_2 is a recently discovered new TMDC material [106]. While ReS_2 shares the most common advantages of TMDCs, such as the X-M-X sandwich structure and ambient stability, two characteristics make it unique. One is the direct band-gap independent of the layer number (1.35–1.43 eV at the GGA level) [104,107], which makes ReS_2 promising for high-efficiency photodetectors [42,108,109]. The other one is anisotropy [110]. Because of this anisotropic nature, it is possible for a ReS_2 transistor to simultaneously possess a large density of states and a large average carrier velocity. Large scale ReS_2 with high crystal quality has been fabricated [111]. A few-μm-length FL ReS_2 FET has been fabricated, showing an on/off ratio up to 10^6 [108].

In the sub-10 nm regime, the zigzag-directed ML ReS_2 MOSFETs are predicted to outperform the armchair-directed devices [100]. Moreover, the ReS_2 MOSFETs with a sub-10 nm gate length along zigzag direction outperform the MoS_2 MOSFETs in the on-state current and have *SS* in the range of 52 to 133 mV/dec, suggesting excellent gate control ability. Such nice electrostatics make the sub-10 nm ReS_2 MOSFETs competitive candidates for the LP applications: their delay time and PDP can satisfy the 2013 ITRS requirements for LP with the gate length scaling down to 3 and 1 nm, respectively.

A common feature from the summarized data in Fig. 3.7(b) is the excellent gate electrostatics of the sub-10 nm ML MX_2 FETs. Due to the stronger short channel effects, *SS* increases as the gate length decreases. However, *SS* of the sub-10 nm ML MX_2 FET remains small (60–110 mV/dec) even when the gate length is only 1 nm. *SS* values below the thermal limit

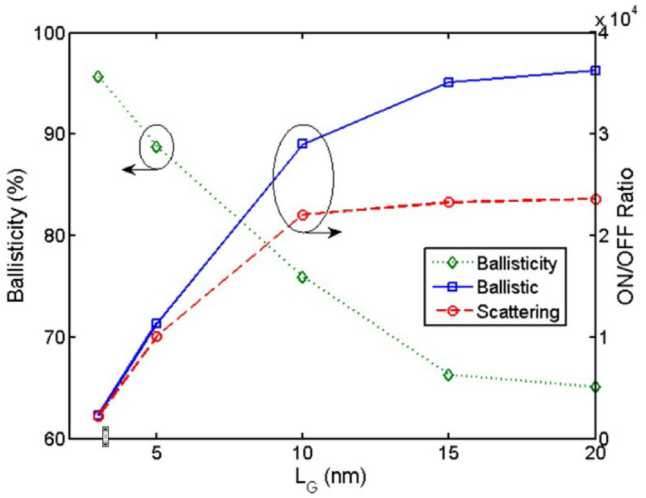


Fig. 3.8. Ballisticity and on/off ratio of the ML MoS_2 FETs versus gate length.
Source: Reproduced from Ref. [70].

of 60 mV/dec are frequently observed. The main reason for such a breakthrough is the contribution of the tunneling current [72]. The total drain to source current comes from the tunneling and thermionic currents ($I = I_{\text{tunnel}} + I_{\text{therm}}$), and SS can be expressed as:

$$SS = (\frac{\partial \lg I}{\partial V_g})^{-1} = (r_{\text{tunnel}} SS_{\text{tunnel}}^{-1} + (1 - r_{\text{tunnel}}) SS_{\text{therm}}^{-1})^{-1} \tag{3.1}$$

where $SS_{\text{tunnel}} = (\frac{\partial \lg I_{\text{tunnel}}}{\partial V_g})^{-1}$, $SS_{\text{therm}} = (\frac{\partial \lg I_{\text{therm}}}{\partial V_g})^{-1}$, and $r_{\text{tunnel}} = \frac{I_{\text{tunnel}}}{I}$, respectively. The lowest limit of 60 mV/dec is set to SS_{therm}. The total SS also suffers from this limit in a device with a long channel since the source to drain direct tunneling is almost neglected ($r_{\text{tunnel}} \approx 0$ and $SS \approx SS_{\text{therm}}$). However, when the device is very short, the tunneling current cannot be neglected ($r_{\text{tunnel}} \neq 0$), and a SS smaller than 60 mV/dec is possible.

The sub-10 nm MX_2 FETs are more suitable as the LP devices than the HP ones. Most of the cases fail to meet the ITRS HP goals for the on-state current and delay time but meet the LP goals. All the sub-10 nm MX_2 FETs show delay time shorter than the ITRS LP goals. Besides, all the sub-10 nm MX_2 FETs show PDP smaller than the ITRS HP and LP standards.

Comparing the sub-10 nm FETs with different MX_2 channels, the ML WSe_2 FETs generally show larger on-state currents and shorter delayer times than the ML MoS_2 and ReS_2 ones. Therefore, a fast switching speed of the WSe_2 FET is expected. MoS_2 is the most commonly studied channel material for the sub-10 nm transistors among MX_2. However, the corresponding transistor's performance is poor as HP devices and merely mediocre as LP devices compared with WSe_2 and ReS_2. The PDP values of the ML ReS_2 FETs are generally smaller than those of the WSe_2 and MoS_2 ones. Though ReS_2 possesses anisotropy, the performance of the ML ReS_2 FETs is not as high as expected from the semi-empirical transport simulation [98]. Such a discrepancy highlights the importance of the *ab initio* quantum transport simulation.

In the experiment, the largest on-state current of the sub-10 nm MoS_2 SBFETs is reported to be 250 μA/μm so far [46–50,92]. The on-state current of the simulated sub-10 nm ML MoS_2 MOSFETs is apparently larger (600 μA/μm). This difference is ascribed to the existence of the Schottky barrier, and actually, the commonly used metal top contact always results in a Schottky barrier for ML MoS_2 both experimentally and theoretically due to the strong Fermi level pinning [67,112]. A possible method to lower the electrical contact barrier is to fabricate 2D/2D contact. *i.e.* apply the 2D metal such as graphene or titanium carbides/nitrides (MXenes) as the source or drain. The advantage of graphene electrodes is the electrically tunable Schottky barrier due to the small density of states near the Fermi level in graphene [113,114]. MXenes might form Ohmic contact with MX_2 because the work function can be tuned on a large scale by surface functionalization [115].

In the actual 2D MX_2 transistors, electron–phonon scattering degrades the carrier transport and thus the current. Therefore, it is important to figure out the difference between the device performances in the ballistic limit and in the real condition. The ballisticity is defined as the ratio between the current with consideration of scattering and the one in the ballistic limit. As shown in Fig. 3.8, the ballisticity of the ultrashort MX_2 FETs increases, and the on/off ratio calculated from the ballistic transport approaches to the one with consideration of the scattering as the channel length decreases. In the ML MoS_2 FETs, the ballisticity reaches 65% at $L_g = 20$ nm, 76% at $L_g = 10$ nm, and nearly 90% at $L_g = 5$ nm, in terms of the semi-empirical simulations by Liu [70]. Hence, for the sub-10 nm gate-length FET with a long channel due to the use of UL structure, the ballisticity is probably decreased to 65%. But for the short channel device, the ballistic transport is a good approximation.

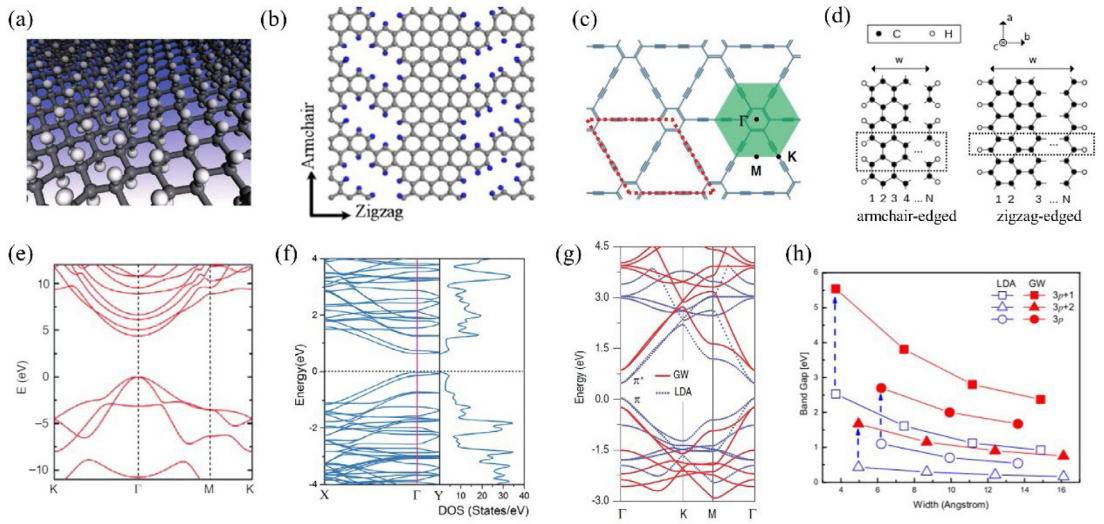


Fig. 4.1. Optimized atomic structures of ML (a) graphane, (b) NPG, (c) GDY, and (d) GNR. Band structures or band-gap of (e) graphane, (f) NPG, (g) GDY, and (h) GNR.
Source: (a) and (e) are reproduced from Ref. [126]. (b) is reproduced from Ref. [127], (c) and (g) are reproduced from Ref. [128]. (d) is reproduced from Ref. [129], (f) is reproduced from Ref. [130]. and (h) is reproduced from Ref. [131].

4. Sub-10 nm group IV FETs

4.1. Fundamental properties of 2D group IV semiconductors

Due to the exceptionally high mobilities of charge carriers in the experiments, graphene is widely regarded as a promising material for next-generation electronic applications [116,117]. However, the lack of an energy band-gap in graphene limits its use in logic applications like FET devices. Although a vertical electrical field [118,119], BN sandwich [120], single-side adsorption [121,122] and substrate [123] can open a band-gap of graphene, the band-gap is generally too small to meet the requirement of a high-performance logic device (greater than 0.4 eV) [38]. For a long time, researchers tried to make the semiconducting form of graphene to realize the high on/off ratio FETs. There are several kinds of graphene-related semiconductors.

The first structure hitting the mind was the hydrogenated graphene, which was called graphane. As one of the graphene derivatives, graphane was firstly synthesized by Elias et al. as early as 2009 [124]. Graphane showed stability at ambient conditions for many days and high charge carrier mobility of about 14000 $cm^2/V{\cdot}s$ in the experiment [124]. The atomic structure of ML graphane is shown in Fig. 4.1(a). The lattice constants are optimized to $a = b = 2.51$ Å. Every carbon atom of the graphane layer is covalently bonded to a hydrogen atom leading to the hybridization change from sp^2 to sp^3 [125]. As a result, a large band-gap of about 3.5 eV is opened in ML graphane at the LDA/GGA level, as shown in Fig. 4.1(e) [126].

Nanoporous graphene (NPG) is another important semiconducting form of graphene, as shown in Fig. 4.1(b). It was firstly synthesized by Moreno et al. in 2018 through bottom-up experimental methods and possessed room-temperature stability [132]. The lattice constants along the zigzag and armchair directions were calculated to be 32.383 Å and 8.534 Å , respectively [130]. The band-gap in NPG is about 0.68 eV at the GGA-PBE level (Fig. 4.1(f)) [130] and about 1 eV in the experiment (acquired from the scanning tunneling spectroscopy spectra) [132]. The theoretical intrinsic carrier mobility is calculated as 800 $cm^2/V{\cdot}s$ due to the low effective mass of about 0.09 m_e in terms of deformation potential theory by Li et al. [133]. Besides, the graphene nanomesh structure built by Duan et al. using O_2 plasma exposure and the periodic holey graphene (HA) structures researched by Yang et al. theoretically can also open the band-gap of graphene [134–137]. Herein, we preferred to discuss NPG material.

Graphdiyne (GDY) is another 2D carbon allotrope containing both sp and sp^2 hybridized carbon atoms in one layer, as shown in Fig. 4.1(c). In 2010, 2D GDY was firstly synthesized by Li et al. and demonstrated good chemical stability [138]. The optimized geometric structure of one kind of GDY is presented with the lattice constants of $a = b = 9.42$ Å [128]. The theoretical intrinsic electron/hole mobility is about 10^4–10^5 $cm^2/V{\cdot}s$ in ML GDY at room temperature based on deformation potential theory [139], which is comparable to that of graphene. Luo et al. found that the band-gap of GDY increases to 1.10 eV within the GW many-body theory from a value of 0.44 eV within the DFT due to the enhanced Coulomb interaction in reduced dimensionality, as shown in Fig. 4.1(g) [128]. The optical band-gap of GDY was also calculated as 0.55 eV within the GW–Bethe–Salpeter equation [128].

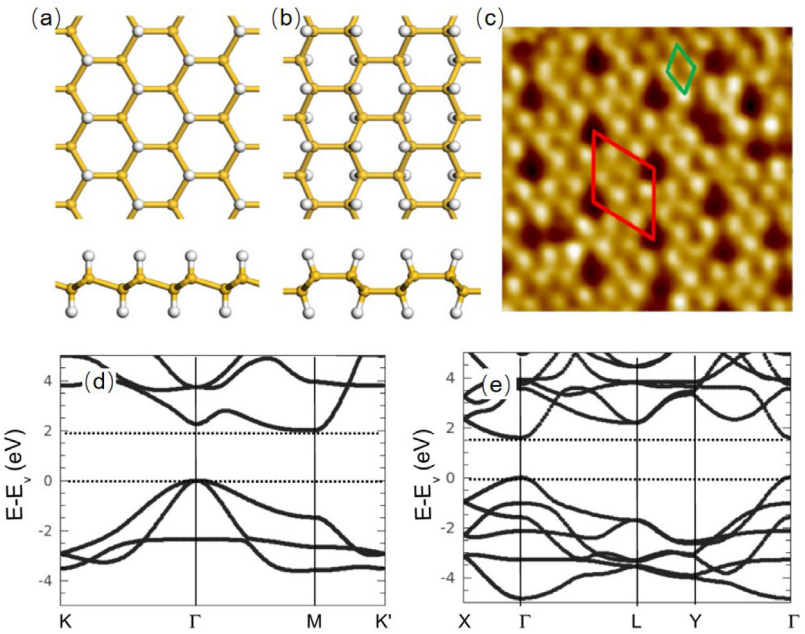


Fig. 4.2. (a) Chair and (b) boat configurations of silicane are shown in side view (lower) and top view (upper). H and Si atoms are represented by white and yellow balls, respectively. (c) STM images of 4.3 × 4.3 cm^2 area of hydrogenated silicene. The (1 × 1) periodicity is indicated by a green diamond, and red diamonds illustrate the ($2\sqrt{3} \times 2\sqrt{3}$) cell with respect to Ag(111) surface. (d, e) Band structures of the chair-like and boat-like silicane.
Source: Reproduced from Ref. [42]. Ref. [146], and Ref. [151].

Besides graphane, NPG, and GDY, another approach to open a band-gap in graphene is to make it narrow to build the graphene nanoribbon (GNR). The quantum confinement effect opens a band-gap in the GNRs. There are two kinds of GNR depending on their direction of edge: armchair-edged GNR and zigzag-edged GNR, as shown in Fig. 4.1(d). The zigzag-edged GNRs are predicted to have smaller band-gaps and electronic states localized along the zigzag edges, which are usually researched as spin-polarized devices [140]. By contrast, the theoretical work shows that the band-gap of armchair-edged GNR increases with the decreased width and can reach a value up to ∼5 eV, as shown in Fig. 4.1(h) [131].

Silicene, silicon analog to graphene, is the 2D structure of silicon. The use of silicene in electronic devices is highly attractive because it is compatible with the existing dominant silicon CMOS technique. However, the gap-less nature limits its application in electronics [42,141,142]. Although its band-gap can be opened by a vertical electrical field according to the calculation in 2012, the maximum band-gap is less than 0.1 eV under an experimentally accessible electrical field [143,144]. The band-gap is predicted to reach 0.5 eV by single-side adsorption of molecules [61]. Experimentally, silicene FET has been fabricated on Ag(111) substrate with a current on/off ratio of 10 in 2015 [145]. The measured electron and hole mobilities are 58 and 129 cm^2/V·s, respectively. However, this FET is extremely unstable under ambient conditions.

Hydrogenation is proved to be an effective method for opening a band-gap of silicene [146]. Silicane, hydrogenated silicene, is the thinnest 2D structure of silicon with semiconductor characteristics. Layered silicane has been successfully synthesized by the reaction of $CaSi_2$ with HCl [147]. Hydrogenated silicene with hydrogen on one side, the so-called half-silicane, are grown on Ag(111) surface, and the band structures of half-silicane are revealed by angle-resolved photoelectron spectroscopy, which is closely reproduced by the theoretical calculations [146,148]. In the DFT calculations, two kinds of stable ML silicane configurations: the boat and chair configurations, are predicted, as shown in Fig. 4.2. The more stable configuration of silicane is the chair configuration according to the DFT calculations [149,150]. The bandgap of chair-like and boat-like silicane is 2.0 eV (indirect) and 1.6 eV (direct), respectively [151]. What is more, small effective masses are predicted in chair-like silicane to be $0.04m_e$ and $0.076m_e$ for the electron and hole carriers, respectively [149]. Compared with other 2D semiconductors, silicane is more compatible with the well-established technology based on silicon. The band gap of silicene can also be opened by the formation of silicene nanomesh and silicene nanoribbons [152–154].

The band gap of zero-bandgap germanene can also be open by vertical electrical [143] and single-side molecule adsorption [155]. Germanane (GeH) is the hydrogenated form of germanene. Its layered van der Waals crystal consists of a hexagonal lattice of germanium atoms with covalently bonded hydrogen atoms. The GeH crystal can be fit to a 2H unit

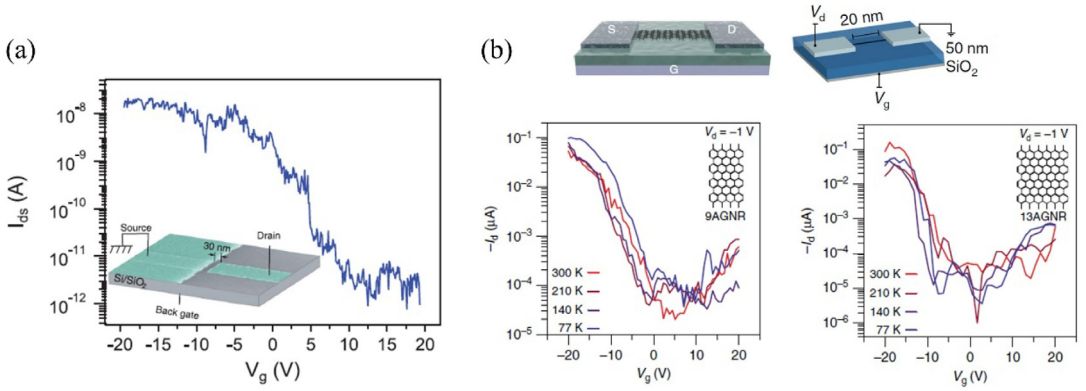


Fig. 4.3. Experimental transfer characteristics of (a) NPG and (b) GNR based FETs.
Source: (a) is reproduced from Ref. [132]. (b) is reproduced from Ref. [159].

cell with $a = 3.880$ Å and $c = 11.04$ Å (5.5 Å per layer). The calculation based on HSE-06 hybrid functional predicts that ML GeH has a direct band-gap of 1.56 eV, whose electron mass is 0.09 m_0 and hole masses are 0.43 m_0 (heavy hole) and 0.10 m_0 (light hole) [156]. The GW band-gap of GeH can be tuned from 2.81 eV to 1.86 eV by controlling the stacking layers from ML to bulk state [151,157]. Another charming result is that the phonon-limited electron mobility can reach up to 18195 cm $^2V^{-1}S^{-1}$ at room temperature, according to the first principal calculations [156].

Like other layered van der Waals crystals, ML and FL GeH can be obtained by mechanical exfoliation. The gram-scale crystals of GeH were synthesized by Bianco et al. for the first time by the topochemical deintercalation of $CaGe_2$ [156]. Bulk GeH shows superior stability in the air: its surface layer gets oxidized slowly in 5 months in exposure to air, while the inner layers resist oxidation. Moreover, GeH is thermally stable up to 75 °C. Amorphization and dehydrogenation start at 75 °C and 200 to 250 °C, respectively. From the diffuse reflectance absorption spectroscopy, the band-gap of GeH was estimated to be 1.59 eV [156].

4.2. Experimental long 2D group IV FETs

The hydrogenated graphene transistor had been reported by Son et al. experimentally in 2016 [158]. It has a hydrogenated graphene channel of 25%H coverage (compared with 100%H coverage of graphane). This FET demonstrated a high on/off current ratio of 3×10^6 for a gate voltage swing of more than 40 V. However, there is little evidence for the intrinsic-graphane-based FET reported in the experiments.

Both NPG and GNR are widely investigated as the channel for the FETs. To build the ML NPG-based FET, NPG was firstly transferred onto a Si/SiO_2 substrate and then contacted with Pd electrodes [132]. The smallest channel length in the ML NPG-based FET is about 30 nm, as shown in Fig. 4.3(a). From the transfer characteristics, it is obvious that ML NPG-based FET shows good performance with a high on/off ratio of 10^4. However, the transfer characteristics are highly nonlinear at low bias, implying the Schottky contact at the Pd–NPG interface. Such interfacial contact properties deserve more effort to improve, and the Ohmic contact is desirable

In the past, many GNR-FETs had been fabricated [160,161]. Herein, we introduce the 9C-armchair-GNR (9AGNR) and 13C-armchair-GNR (13AGNR) based FETs reported by Llinas et al. in 2017 [159]. The 9AGNR and 13AGNR based FETs were fabricated with a nominal 20 nm channel length and a 50 nm SiO_2 gate dielectric, as shown at the top of Fig. 4.3(b). Pd metal is used as the electrode in the FETs. From the nonlinear behavior at low bias in the transfer characteristics, the interfacial Schottky contacts are also observed. The weak temperature dependence in the transfer characteristics suggests that the limiting transport mechanism is tunneling through the barrier as opposed to thermionic emission over the barrier at the contacts in the 9AGNR and 13AGNR-based FETs. Furtherly, by introducing thin HfO_2 solid dielectric gates to 9AGNR-FETs, the device exhibits better switching characteristics, which demonstrates a high on/off current ratio of about 10^5 and I_{on} of about 1 μA at $V_d = -1$ V [159].

The first 2D germanane FETs, whose thicknesses range from 15 nm to 90 nm, were fabricated by Madhushankar et al. [162]. The electronic transport characteristic experiments show a high on/off current ratio of 10^5 (10^4) at 77 K (room temperature) in both electron-doped and hole-doped regimes. The four-terminal electrical measurement at room temperature gives carrier mobility of ∼30 cm^{2}V^{-1}S^{-1} for both electron and hole, and the two-terminal measurement gives the hole mobilities of 150 cm^{2}V^{-1}S^{-1} below 150 K and 70 cm^{2}V^{-1}S^{-1} at room temperature. Under the illumination of 650 nm laser, there is a significant enhancement of the FET conductivity.

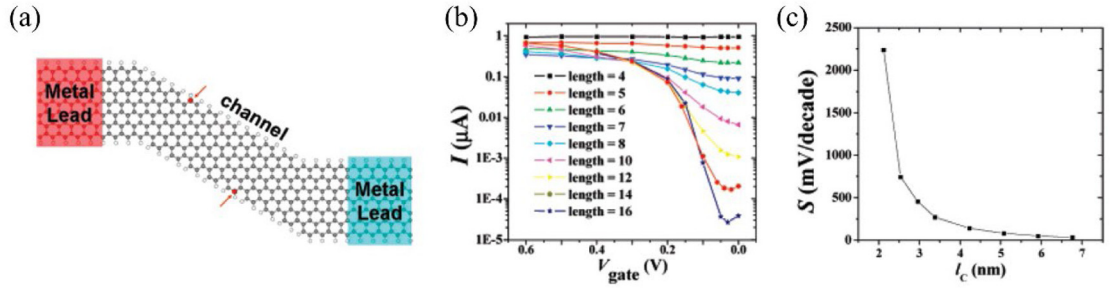


Fig. 4.4. GNR-FET: (a) Schematics of the model, (b) Transfer characteristics as a function of the channel length, and (c) Subthreshold swing as a function of the channel length.
Source: These figures are reproduced from Ref. [163].

4.3. Simulation of sub-10 nm 2D group IV FETs

As early as 2007, Duan et al. had simulated the patterned GNR based FET (Fig. 4.4(a)) [163]. Such a FET structure is made from one armchair-edged semiconducting GNR channel with two zigzag-edged metallic GNR leading connected to two external metal electrodes. As shown in Fig. 4.4(b), the transfer characteristics of the GNR-FETs with the varying channel length from 1.69 to 6.76 nm are simulated. Herein, the V_b is set as 20 mV. *SS* of the GNR-FETs decreases with the increasing channel length and gradually approaches 60 mV/decade when the channel length becomes longer than 6 nm, as shown in Fig. 4.4(c). The 6 nm-channel-length GNR-FET also demonstrates an on/off current ratio of about 10^3–10^4. However, the *ab initio* quantum transport simulation results are not benchmarked against the requirements of ITRS for the sub-10 nm GNR-FETs.

The sub-10 nm ML GDY transistor had been examined ed by Pan et al. [164] and Sang et al. [165] through the *ab initio* quantum transport simulations. Pan et al. predicted that the ML GDY-based FET with Al electrodes possessed a high on/off current ratio of 10^4 and I_{on} of 1.3×10^4 μA/μm in a 10 nm channel length due to the interfacial Ohmic contact. In Sang et al.'s work, the UL structure is abandoned in the ML GDY-based FET because Sang et al. thought that UL architecture fails to downscale the actual size of the devices. After the systematic research, it was found that pristine ML GDY-FET can be scaled down to 7.3 nm with I_{on} meeting the requirement of ITRS for the HP devices. In this length of the channel, I_{on} reaches 1264 μA/μm. By introducing the strain engineering to the ML GDY-based FET, the performance could be furtherly improved. The strained-engineered 8.8 nm-channel ML GDY FET could fulfill the requirement of ITRS for both the HP and LP application. The *SS* was also reduced by 15%–37% due to the strain engineering, implying a better gate-control ability.

As shown in Fig. 4.5, both the optimized *n*-type and *p*-type ML chair-like silicane MOSFET can well or nearly meet the ITRS HP requirement for I_{on}, τ, and PDP at $L_g = 5$ nm according to the *ab initio* quantum transport simulation [166]. The optimized *n*-type ML chair-like silicane MOSFET at $L_g = 3$ and 5 nm and *p*-type one at $L_g = 5$ nm can meet the ITRS LP demand for I_{on}, τ, and PDP. The optimized on-state current of the *n*-type ML chair-like silicane HP MOSFET at $L_g = 5$ nm is 1374 μA/μm, which is twice larger than that of its ML MoS_2 counterpart ($L_g = 598$ μA/μm) and comparable to that of its ML InSe counterpart [166]. The optimized effective delay time and PDP of the *n*-type and *p*-type ML silicane MOSFETs can well meet the HP and LP device requirement of the ITRS until $L_g = 1$ nm. We note that large on-state currents in the silicane FETs are also predicted by the semi-empirical methods [167,168].

Compared with the experimental ultra-thin-body Si-on-insulator (UTB SOI) FETs [169], the theoretical ML silicane FETs show a larger on-state current (258 μA/μm for the silicane FET *vs.* 100 μA/μm for the experimental UTB SOI FETs at $V_{dd} = V_g = 0.5$ V). The larger on-state current of the ML silicane FETs is attributed to its small thickness of 0.37 nm and few interfacial traps between the silicane layer and dielectrics. Such a tiny thickness of the silicane layer leads to a small characteristic length of $\lambda = 0.49$ nm for the DG silicane FET. By contrast, the thickness is 8 ± 2 nm in the experimental UTB SOI FETs, and the corresponding characteristic length is $\lambda = 1.99$–2.57 nm.

In addition to UTB SOI FET, FinFET is another representative advanced Si FET structure. The experimental Si FinFETs also show performance degradation at the sub-10 nm-L_g region. The measured on-state currents of the tri-gate FinFET at $L_g = 10$ nm and GAA FinFET at $L_g = 5$ nm are only 110 and 252 μA/μm at $V_{dd} = 0.6$ V, much lower than the HP standard required by the ITRS [2]. Such a poor performance of the experimental sub-10 nm-L_g Si FinFETs is ascribed to the large fin width ($W_{Fin} > 3$ nm). Based on a newly developed atomic layer etching and atomic layer deposition (ALE-ALD) method, an InGaAs FinFET with a very small fin width of $W_{Fin} = 2.5$ nm was successfully synthesized [171]. Lately, the ML MoS_2 FinFET with a smaller $W_{Fin} = 0.6$ nm was also fabricated by a developed template-growth method [172]. These technological advances have shed light on the realization of the narrower Si FinFETs.

A UTB Si FinFET (Fig. 4.5(b)) with $W_{Fin} = 0.8$ nm is investigated based on the *ab initio* quantum transport simulations [170]. Such a 5 nm-L_g UTB Si FinFET can still meet the ITRS 2013 HP requirements in terms of the on-state current, delay time, and power dissipation when the perfect structure is kept [2,170]. The calculated HP I_{on}, τ, and PDP of the 5 nm-L_g UTB Si FinFET are comparable with those of the 5 nm-L_g ML silicane MOSFET (Fig. 4.5(c)). The UTB Si FinFET for the LP

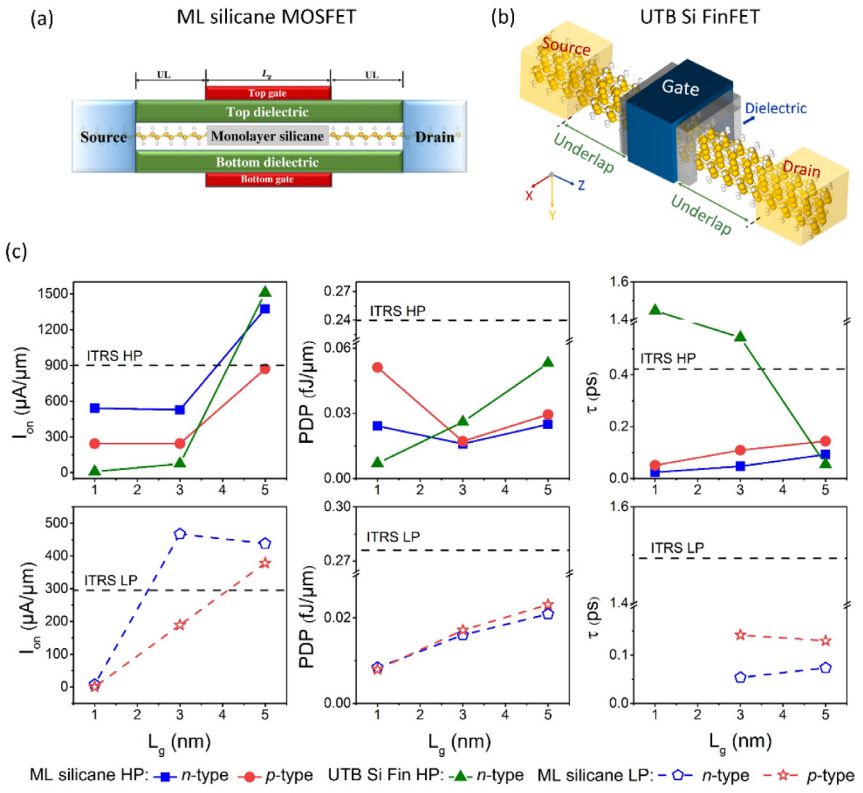


Fig. 4.5. Schematic diagrams of (a) the ML chair-like silicane MOSFET and (b) the UTB Si FinFET. (c) Benchmark of the optimal on-state current, PDP, and delay time versus L_g for the *n*- and *p*-type sub-5 nm ML silicane HP/LP MOSFETs and the *n*-type sub-5 nm HP UTB Si FinFETs.
Source: (a) is reproduced from [166]. (b) is reproduced from [170].

application is not considered because of the large leakage current. The defect's influence on the UTB Si Fin devices is also investigated (Fig. 4.6). In the perfect device, the on-state transmission eigenstates ($E = 0.32$ eV and $\boldsymbol{k} = (0, 0)$) transport from the drain to the source with very little loss, and the calculated I_{on} is 351 μA/μm. With the defect concentration increasing to 0.6% and 1.2%, the transmission eigenstates at the given energy decay sharply, and the corresponding I_{on} decrease rapidly to 249 and 54 μA/μm (Fig. 4.6(a) and (c)), respectively. Therefore, structural integrity is critical to keep the good device performance of the UTB Si FinFETs.

Atomistic quantum transport simulations based on NEGF within tight-binding approximations were used to characterize the properties of sub-10 nm ML germanane FETs [173]. The *SS*, DIBL, and V_{th} of the ML germanane FET with a channel length of 6 nm (10 nm) and a proper electron doping concentration of 5.5×10^{12} cm^{-2} are 175 mV/dec (88 mV/dec), 272 mV/V (109 mV/V), and 0.775 V (0.875 V), respectively [173]. For the ML germanane FET with a channel length of 10 nm, the highest on/off ratio can reach 10^5 with an on-current of ~70 μA/μm.

More accurate *ab initio* quantum transport simulation is expected for the ML sub-10 nm ML germanane FETs. Besides, *ab initio* quantum transport simulation is also desirable for the sub-10 nm FL silicane and germanane FETs since they can more represent the sub-10 nm UTB Si and Ge FETs. Investigation of the device scaling behavior with the channel thickness is an interesting and useful direction for the sub-10 nm FETs.

5. Sub-10 nm group V FETs

5.1. Fundamental properties of 2D group V-enes

In 1914, Percy Bridgman synthesized black phosphorus (BP) from red phosphorus at high pressure and temperatures [174]. BP is a layered material, and each layer has a puckered orthogonal structure (α phase). The discovery of graphene makes BP regain intense interest, and the 2D form of BP, termed black phosphorene (abbreviated to BP too), has been fabricated in 2014 [175,176]. Later, a few 2D phosphorus analogs have been predicted [177–180]. ML blue phosphorene (abbreviated to BlueP) with a buckled hexagonal structure (β phase) has been fabricated on Au(111) [181] or tellurium functionalized Au(111) [182] in quick succession. ML BP (α phase) is energetically more stable than BlueP (β phase). 2D As and Sb, termed as arsenene and antimonene, also possess stable α phase (puckered) and β phase (buckled) similar

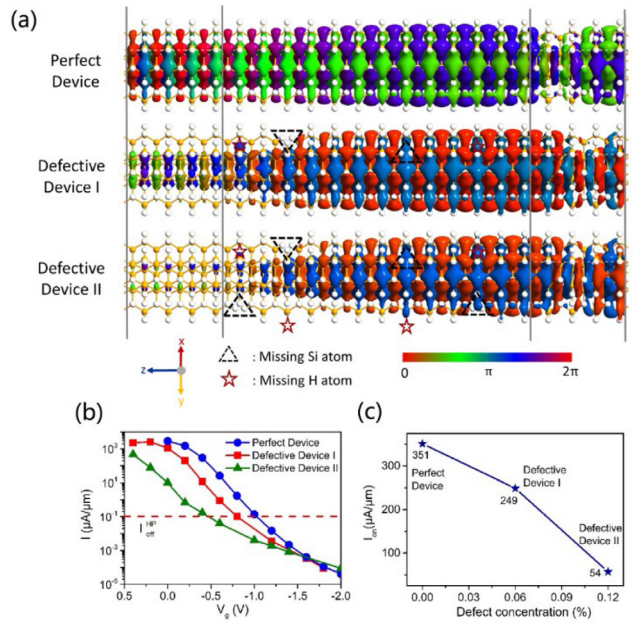


Fig. 4.6. Defect's influence on the UTB Si FinFET. (a) On-state transmission eigenstates ($E = 0.32$ eV and $\boldsymbol{k} = (0, 0)$) of the perfect device, defective device I (defect concentration of 0.6%), and defective device II (defect concentration of 1.2%) with $L_g = 5$ nm and $L_{UL} = 0$ nm under $V_{bias} = 0.64$ V. The iso-value is 0.02 a.u. The phase color scale is shown under the plot. (b) Transfer characteristics. (c) On-state current as a function of the defect concentration.
Source: Reproduced from Ref. [170].

to phosphorene [183], but the β phase is energetically favored [184]. In the following, we discuss the most energetically stable phase α phase BP, β phase arsenene, and β phase antimonene unless otherwise specified.

As shown in Fig. 5.1(a–d), 2D BP is a direct semiconductor, and its bandgap ranges from 2 eV for ML to 0.3 eV for bulk form [185]. The spin–orbital coupling (SOC) is found to have no appreciable effect on the electronic structure of BP [185]. An interesting characteristic of BP is its electronic anisotropy [28,185]. The effective mass of ML BP in the armchair direction is much less than that in the zigzag direction for both electrons ($m_x = 0.17m_0$ *vs.* $m_y = 1.12m_0$) and holes ($m_x = 0.15m_0$ *vs.* $m_y = 6.35m_0$). Correspondingly, the carrier mobilities along the zigzag direction are 180 and 400 $cm^2/V{\cdot}s$ for hole and electron, respectively. In contrast, those along the armchair direction reach up to 2770 and 800 $cm^2/V{\cdot}s$ for hole and electron, respectively [186].

By employing the GW approximation and *ab initio* many-body Green's function (Fig. 5.1(e–f)), researchers predicted that the bandgaps of ML hexagonal (β phase) antimonene and arsenene to be 2.38 and 2.47 eV, respectively [60]. Calculated at room temperature (300 K), the hole (electron) mobilities under intrinsic acoustic phonon-limited conditions are approximately 510 (150) and 66 (21) $cm^2/V{\cdot}s$ for ML antimonene and arsenene, respectively. While employing the deformation potential theory, hole/electron mobilities for ML hexagonal antimonene and arsenene (1700/635 and 1737/630 $cm^2/V{\cdot}s$) are predicted to be dozens of times higher [187]. A possible reason for such overestimation might be the inconsideration of the ZA phonons.

5.2. Experimental long black phosphorene and black arsenene FETs

Up to now, BP [188–190] and β phase antimonene [191–193] can be fabricated down to a single layer by molecular beam epitaxy, van der Waals (vdW) epitaxy, liquid-phase exfoliation, mechanical exfoliation, or epitaxial growth. Arsenene (β phase) has been fabricated in the experiment by aqueous shear exfoliation [194] or liquid exfoliation [195]. The fabrication of ML arsenene has not been reported yet, but the few-layer nanosheet can be synthesized by plasma-assisted or shear exfoliation.

The high mobility makes BP suitable for electronic applications. Soon after the mechanical exfoliation of BP, several experimental groups fabricate the prototype transistors with BP channel [66,175], demonstrating good device performances (Fig. 5.2). The channel length of the BP transistors so far can be fabricated down to 20 nm through an angle evaporation process, and an on/off current ratio of 100 is reported [196].

Remarkably, ML and FL black arsenene (α phase) are also exfoliated from the natural mineral by Wei et al. [197]. In the ML limit, the black arsenene FET with a channel length of 2 μm shows carrier mobility of 51 $cm^2/V{\cdot}s$ and large on/off ratios of 10^5 (Fig. 5.3). In contrast to 2D BP, 2D black arsenene has relatively good ambient stability. The FL black arsenene FET still works after exposure to air for about one month.

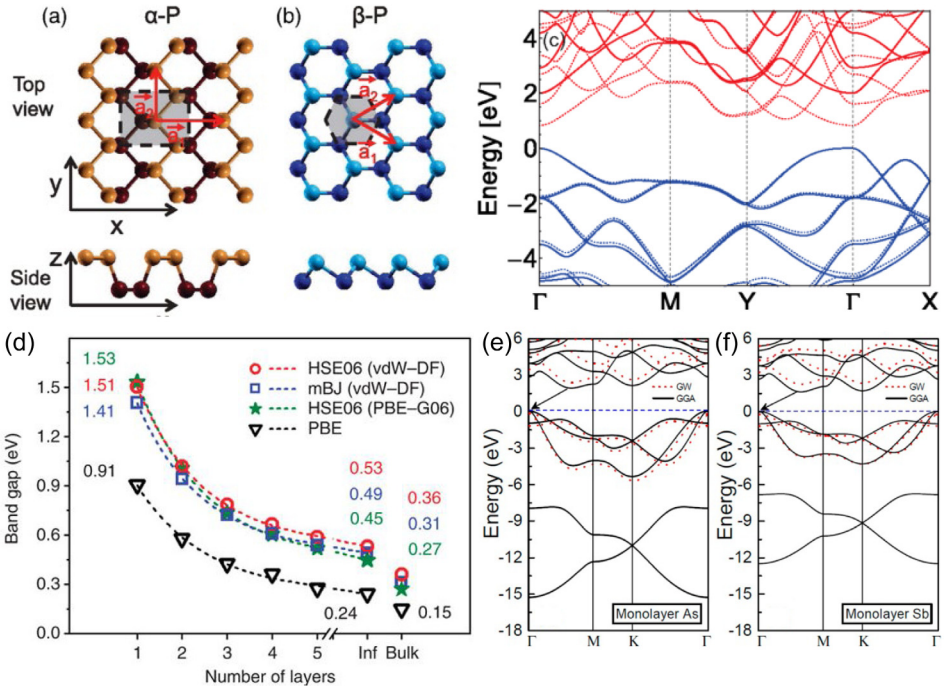


Fig. 5.1. (a–b) Structures of the α phase and β phase of phosphorene [177]. (c) DFT-calculated (dash lines) and GW-calculated (solid lines) band structures of ML BP (α phase). The top of the valence band is set to be zero [185]. (d) Direct bandgaps versus thickness. (e–f) Band structures of ML arsenene and antimonene.
Source: Reproduced from Ref. [177], Ref. [185] and Ref. [60].

5.3. Simulation of sub-10 nm ML phosphorene, arsenene, and antimonene FETs

A noticeable feature of the group V-enes is their anisotropic electronic structures. This anisotropy shows direct effects on the device performance. Although the mobility of BP in the armchair direction is much higher and the effective mass is much smaller than those in the zigzag direction, a higher on-state current of ML BP transistor in the zigzag direction is predicted when the gate length is less than 5 nm according to the *ab initio* quantum transport simulation of Quhe et al. [72]. This phenomenon highlights the importance of suppressing the source to drain tunneling in the ultrashort scale. Unlike the long channel case in which high mobility (and thus a small effective mass) is desired to maximize the on-state current, the channel material with a medium effective mass is suggested for the sub-10 nm transistors to balance high mobility and low tunneling leakage. A high on-state current up to the order of magnitude of 1000 μA/μm is predicted in the ML BP MOSFETs with a gate length less than 5 nm (Fig. 5.4(a)). Even when L_g is scaled to 2/3 nm, the ML BP MOSFETs still surpass the ITRS HP/LP standards for the on-state current, delay time, and power dissipation indicator [72].

The experimental fabricated BP transistor is usually in the form of SBFET, in which a metal–semiconductor contact exists in the source and drain. A Schottky barrier might appear in the electrical contacts. On the other hand, the MOSFET source and drain are highly doped semiconductors, and no Schottky barrier exists. Therefore, a BP transistor model considering electrical contacts might capture some physics that a MOSFET cannot. A comparative study of sub-10 nm ML BP transistors with different electrode materials reveals the electrode materials' apparent effects on the device performance [199]. Compared with bulk metal Ni and Ti, 2D metals such as graphene render better gate electrostatics in the sub-10 nm BP transistor due to the weak electric field screening and tunable Schottky barrier. With graphene electrodes, the sub-10 nm ML BP SBFET could achieve an on-state current of about 90% of the MOSFET.

Wang et al. [198] found that all the studied sub-10 nm BlueP MOSFETs can meet the HP on-state current requirement of ITRS by using the *ab initio* quantum transport simulation. Moreover, the ML BlueP MOSFET outperforms its antimonene, arsenene, and InSe counterparts, in terms of the on-state current. The electron–phonon scattering in the ML BlueP MOSFET with $L_g = 10.2$ nm and UL = 0 leads to the degradation of I_{on} by 25.4% and 23.6% for the HP and LP applications, respectively (Fig. 5.4(b)). However, the phonon-corrected I_{on} still exceeds the ITRS standard greatly. For practical applications, the main factor to limit the lower carrier mobility includes interfacial Coulomb scattering originated from dangling bonds, gaseous adsorbates, impurity scattering, and other nonideal factors.

It is predicted that the ML hexagonal antimonene and arsenene MOSFETs (β phase) can meet the ITRS standards for HP (LP) down to 5 (4) nm gate length [60,200]. The on-state current of the ML hexagonal antimonene and arsenene MOSFETs behave better than that of the ML MoS_2 SBFETs (Fig. 5.5). The 5–7 nm gate-length ML antimonene and arsenene DG

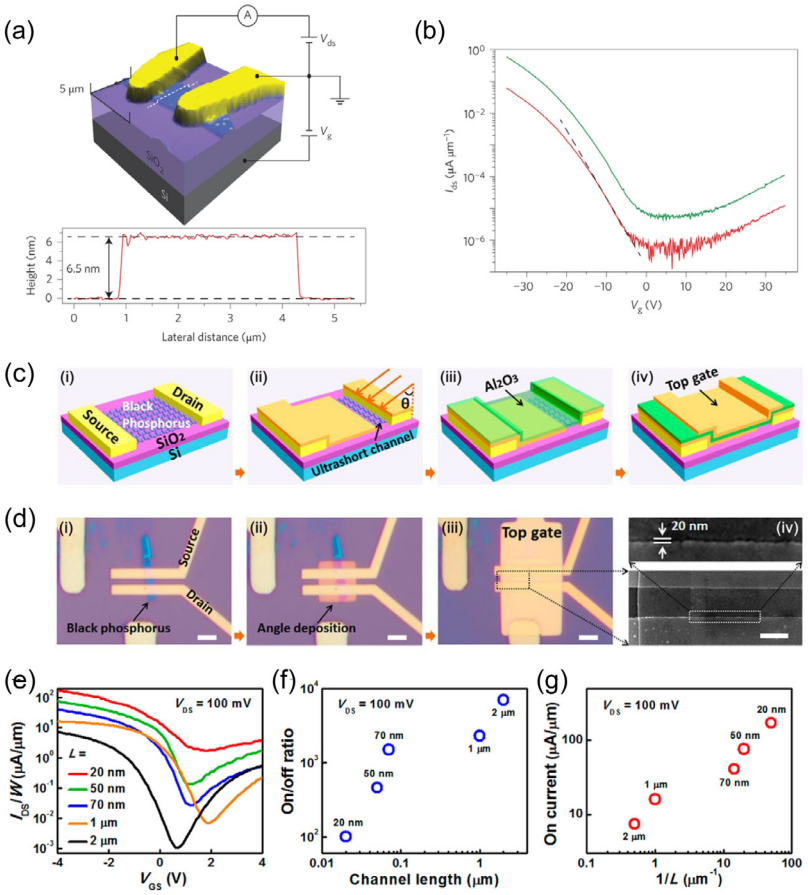


Fig. 5.2. BP-based field-effect transistor. (a) Device structure and device profile of an FL BP FET. (b) Transfer characteristics of a 5 nm-thick device under bias voltages of 100 mV (green curve) and 10 mV (red curve), respectively. (c) BP FETs with an ultrashort channel length are fabricated step by step in the schematic. (d) Corresponding steps under optical microscope and SEM. (e) Transfer characteristics of the BP FETs with top-gate at different channel lengths. (f, g) On/off ratios and on-state current densities as a function of the channel length.
Source: (a, b) are adapted with permission from Ref. [176], and (c–g) are adapted with permission from Ref. [196].

MOSFET are also studied using the semi-empirical method, and the calculated on-state currents of the ML DG antimonene and arsenene MOSFETs are larger than those from the accurate *ab initio* method by a factor of 1.5–2.5 [187].

A noticeable problem of BP for practical applications is its environmental instability [201,202]. Encapsulation of BP with other materials such as hexagonal boron nitride or aluminum oxide is useful for overcoming ambient degradation [175,203–205]. The excellent performance of the ML hexagonal antimonene and arsenene has not been observed experimentally. The bandgap of hexagonal arsenene and antimonene is strongly dependent on their thickness, which is sharply decreased to zero (metallic) as the thickness is increased to TL and BL, respectively [206]. Therefore, fabrication of the ML hexagonal antimonene and arsenene MOSFETs requires the channel thickness's precious control, which undoubtedly raises the difficulty.

Isoelectronic ML GeSe shares many similar properties with ML BP, such as the puckered layered structure (Fig. 5.6(a)), sizable direct bandgap (1.1–1.2 eV) (Fig. 5.6(b)), high carrier mobility ($\sim 10^3$ cm^2/V·s), and electronic anisotropy [207–212]. The fabricated GeSe nanosheet FETs with Cr/Au electrodes have an on/off current ratio of 10^3 [213]. More importantly, unlike BP, ML GeSe shows excellent air stability [213].

By using *ab initio* quantum transport simulation, Guo et al. found that with the aid of UL, I_{on}'s of the sub-5 nm ML GeSe *p*-MOSFETs can meet the ITRS HP standards along the zigzag direction even at $L_g = 1$ nm [214] and are comparable with or higher than those of the BP MOSFETs at $L_g = 1$–3 nm (Fig. 5.6(c)). Along the armchair direction, I_{on}'s of the sub-5 nm ML GeSe *p*-MOSFETs are far below the ITRS HP standard. Such a significant difference is ascribed the obvious smaller hole effective mass along the zigzag direction ($0.11m_0$ along the zigzag direction *vs.* $0.30m_0$ along the armchair direction). We believe that 2D GeSe (including other 2D group IV–VI 2DSCs) is a potential successor of BP in light of the comparable high performance but good ambient stability.

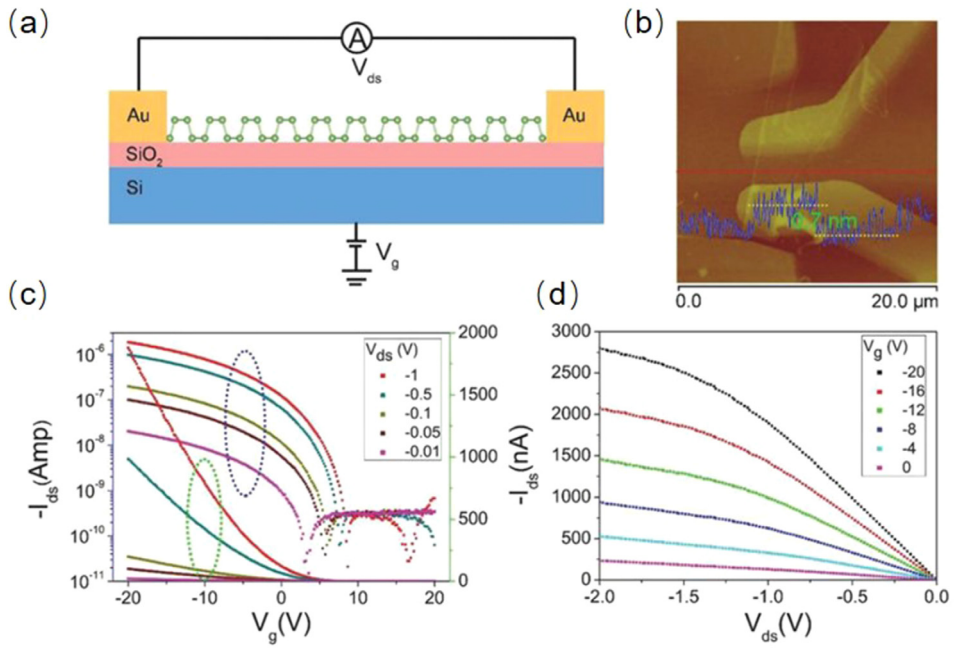


Fig. 5.3. Characterization of ML black arsenene FET. (a) Cross-section of an ML black arsenene FET. (b) Atomic force microscopy (AFM) image of a typical as-fabricated ML black arsenene FET. (c) Transfer curves (I_{ds}–V_g) of the ML device with different drain–source voltage (from −0.01 to −1 V) (d) Output characteristics of the same device.
Source: Reproduced from Ref. [197].

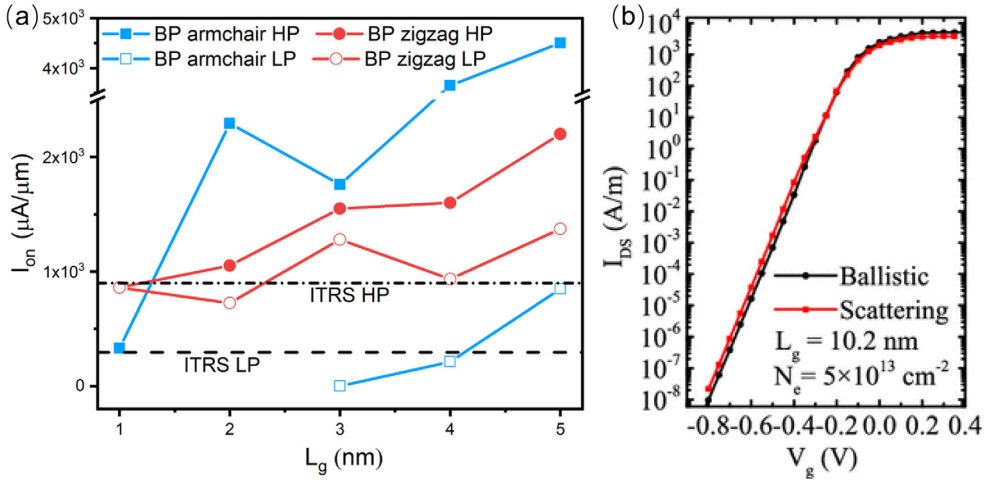


Fig. 5.4. (a) HP and LP on-currents for the ML DG BP MOSFETs. Black dashed lines are the requirements for the HP and LP applications in ITRS 2013. (b) Comparison of the ballistic and scattering current in the 10 nm-gate-length BlueP FET.
Source: (a) Reproduced from Ref. [72]. (b) Reproduced from Ref. [198].

6. Sub-10 nm group III–VI conventional FETs

6.1. Fundamental properties of 2D group III–VI semiconductors

According to stoichiometry, 2D layered group III–VI compounds can be classified into two main categories: MX and M_2X_3 (M = Ga, or In; X = S, Se, or Te). The most intensively studied M_2X_3 is In_2Se_3 of α-phase [216–220]. 2D α-In_2Se_3 has room-temperature ambient stability and a bandgap of about 0.82 eV based on the GGA-PBE level for its monolayer [216,219–223]. Both in-plane and out-of-plane room-temperature ferroelectricity have been found in 2D α-In_2Se_3, making it an excellent candidate for non-volatile memory applications [216,219,220,222,223]. Especially due to

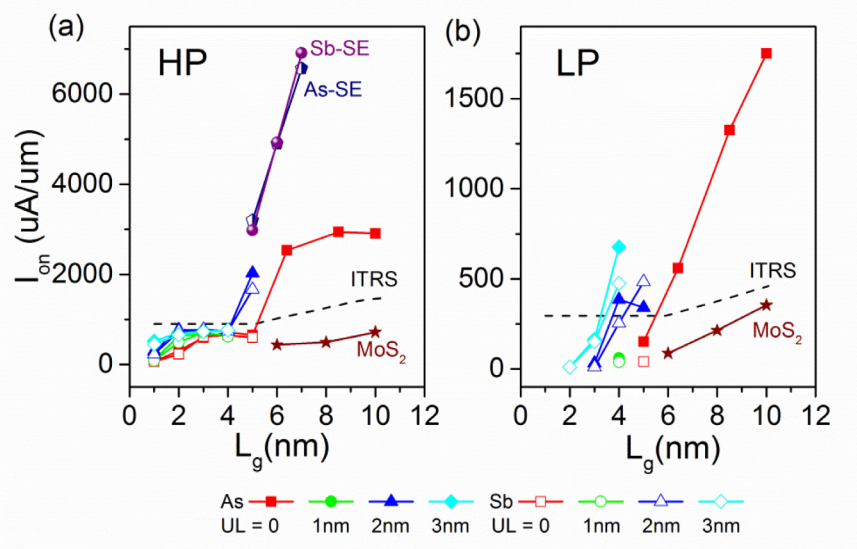


Fig. 5.5. (a) HP and (b) LP on–currents for ML DG hexagonal antimonene and arsenene MOSFETs. Black dashed lines are the requirements for HP and LP applications in ITRS 2013. For comparison, the simulation results of ML DG MoS_2 SBFET with Ti electrodes are shown [96]. As (Sb)-SE [187] represents the values of the SE-NEGF method.
Source: Adapted from Refs. [60,200].

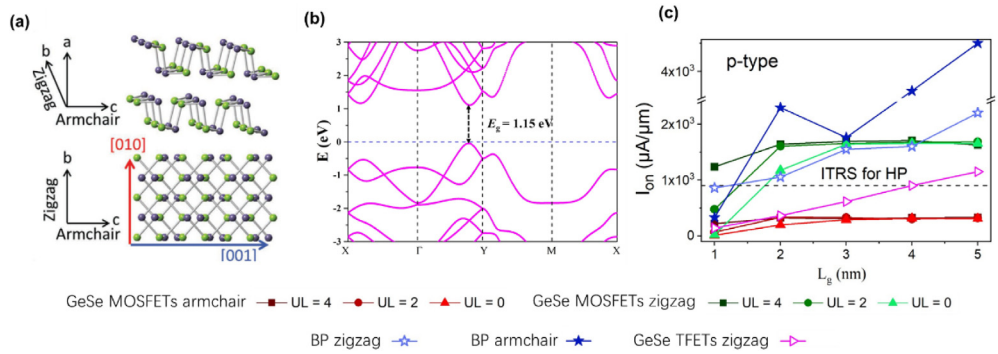


Fig. 5.6. (a) Crystal structure and (b) band structure of ML GeSe. Γ-X and Γ-Y represent the armchair and zigzag direction, respectively. (c) On-state currents of the sub-5 nm DG *p*-type ML GeSe MOSFETs as a function of the gate length. The red and green lines indicate the armchair and zigzag directions, respectively. The on-state current of the optimal simulated *p*-type sub-5 nm DG ML BP MOSFETs (armchair- and zigzag-directed) and ML GeSe TFETs are also shown for comparison and indicated by two blue and magenta symbols.
Source: Adapted from Refs. [72,213,215].

its out-of-plane ferroelectricity (which induces the built-in electric field), the planar-direction-dependent properties of α-In_2Se_3 based heterostructures had been widely researched [220,221,224]. But herein, we mainly focus on MX and their applications for conventional transistors.

MX possesses the common merits of 2D materials and additional advantages, such as high carrier mobility, direct bandgap, and rare *p*-type electronic behaviors [225]. Take InSe as an example. Each InSe layer consists of quaternary Se-In-In-Se atomic sheets connected by intralayer covalent bonding. Bulk InSe has four types of crystal forms, named β, ε, γ, and δ-phases, according to the stacking arrangements of the quaternary layers bonded by interlayer vdW interaction. The atomic structure of ML InSe is shown in Fig. 6.1(a) with the lattice parameters of $a = b = 4.09$ Å [226]. As the layer number increases, the bandgap of 2D InSe decreases from 1.44 (ML) to 0.68 eV (five layers) based on the previous GGA-PBE calculations [226], as shown in Fig. 6.1(b). The band structures of ML InSe were also calculated with GW (indirect bandgap: 2.60 eV), HSE (indirect bandgap: 2.14 eV), and GGA approaches, as shown in Fig. 6.1(c) [227]. Herein, in the center of the Brillouin zone, the valence band is nearly flat, so that the holes are heavy (2.6 m_0 at ML) and the density of states is high, and there are van Hove singularities like sharp peaks at the Fermi level. The electron mass is much smaller (0.24 m_0 at ML) and leads to electron mobility as high as the order of magnitude of 10^3 $cm^2/V{\cdot}s$ [228,229], which is comparable to phosphorene and much higher than MoS_2. One shortcoming of 2D InSe is its instability in the air, and thus a cover of *h*BN is needed for protection [229]. By contrast, its allotrope, 2D α-In_2Se_3 has room-temperature ambient

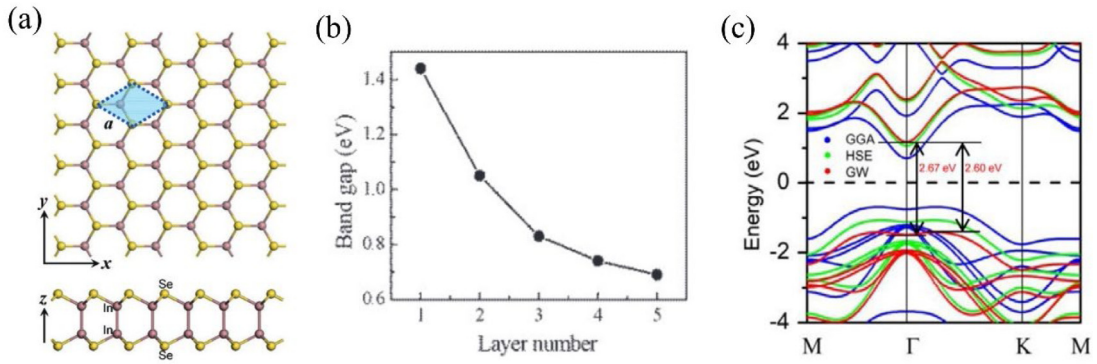


Fig. 6.1. (a) Schematic of the 2D InSe atomic structure. (b) Layer-number dependent bandgaps of 2D InSe. (c) Band structures of ML InSe with GW, HSE, and GGA approaches.
Source: (a) and (b) are adapted from Ref. [226]. (c) is adapted from Ref. [227].

stability [216,219,220,222,223]. Other isoelectric MX materials like GaS and GaSe share similar geometric and electronic properties with InSe [230].

6.2. Experimental long 2D group III–VI FETs

To our knowledge, sub-10 nm group III–VI transistors have not been fabricated so far. Here, we summary some experimental group III–VI conventional FETs with a long channel. Multilayer InSe back-gated FETs with long channel length using PMMA/Al_2O_3 dielectric exhibit a high current on/off ratio of 10^8, robust current saturation, and a high room temperature electron mobility up to 10^3 $cm^2/V{\cdot}s$ [228,231]. The electron mobility is comparable to the strained silicon thin film and higher than that of MoS_2. The FETs based on ML InSe are sandwiched between *h*BN layers and use FL graphene as electrodes. However, the device's on/off current ratio is only 10^2, which may be caused by the electrode contact resistances [229]. ML GaS and GaSe on SiO_2/Si substrate showed typical *p*-type and *n*-type conductance, respectively [230]. The transistors based on ML GaS and GaSe showed good on/off current ratios of 10^4–10^5 and field-effect mobilities of 0.1 and 0.6 $cm^2/V{\cdot}s$, respectively [230]. These low field-effect mobilities might be caused by the surface traps and impurities in the bottom gate dielectric.

It is worth noting that a new ferroelectric semiconductor FET (FeS-FET) had been reported very recently based on the 2D α-In_2Se_3 by Ye et al. [232] and Zhou et al. [233]. Such ferroelectric 2D α-In_2Se_3 was used as the semiconductor channel instead of the ferroelectric insulator (like NCFET), as shown in Fig. 6.2(a). The experimental sample of this device is shown in Fig. 6.2(b). Ye et al. selected 15 nm-thick HfO_2 (or 90 nm-thick SiO_2) as a scaled gate dielectric and the 1 μm-length 2D α-In_2Se_3 as the channel. The atomic layer deposition of the 10 nm-thick Al_2O_3 was also developed to protect and enhance the performance of the FeS-FET. The two nonvolatile polarization states in the FeS-FET lead to a high-quality amorphous gate insulator. Furthermore, the depolarization field across the α-In_2Se_3 was screened by the mobile charges (Fig. 6.2(a)), which greatly eliminates the charge trapping and leakage current through the insulating layer. Finally, the fabricated devices demonstrate high performance with a high on/off ratio of over 10^8 and a high maximum I_{on} of 862 μA μm^{-1} under a low supply voltage, as shown in Fig. 6.2(c). Their findings point to the new direction of group III–VI compounds with the M_2X_3 category.

6.3. Simulation of sub-10 nm ML InSe FETs

The ML InSe based FETs demonstrate promising performance in the sub-10 nm length region, according to the previous theoretical work. The optimal I_{on} of the ML InSe HP and LP MOSFETs at different L_g are shown in Fig. 6.3 [60]. The *n*-type ML InSe MOSFETs have larger on-state current for the HP applications, while the *p*-type ones have larger on-state current for the LP applications. Without the aid of a UL structure, the *n*-/*p*- type ML InSe MOSFETs can fulfill the ITRS HP and LP standards down to 5/3 and 7/5 nm, respectively. Further scaling to 2 nm can be achieved by utilizing a 1–2 nm long UL structure. The quite different effective masses of electron (0.24 m_0) and hole (2.6 m_0) in ML InSe are responsible for this discrepancy for the *n*- and *p*-type devices. ML GaSe is also suitable for sub-3 nm *p*-type HP devices according to a tight-binding combined NEGF simulation [234].

The above performance of ML InSe and GaSe devices is achieved with Ohmic electrode contact as the precondition, and the Schottky barrier that existed between the metal electrode and 2D channel will inevitably deteriorate the on-current [12]. According to the first-principles quantum transport simulations [235–237], Ag, Cu, and In electrodes can form Ohmic contact with ML InSe, and Cu and Ag form Ohmic contact with BL InSe. These electrodes can be adopted in the future 2D InSe device designs.

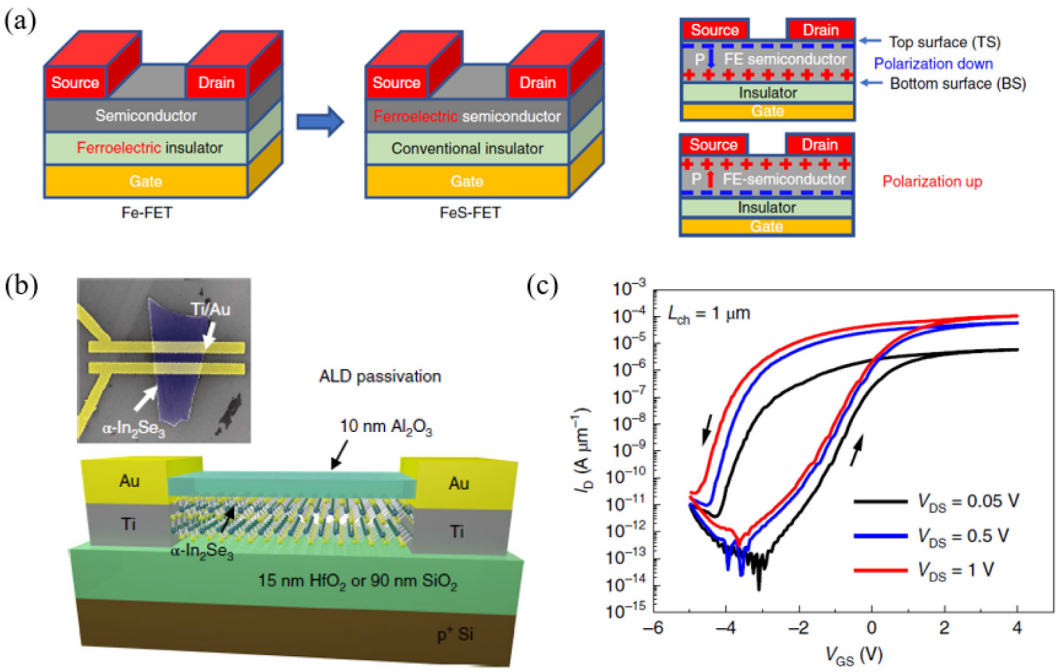


Fig. 6.2. (a) Schematic diagram and polarization bound charge distribution in a FeS-FET in two polarization states. (b) Schematic of the experimental α-In_2Se_3 FeS-FET. (c) I_D–V_{GS} characteristics at room temperature of a representative α-In_2Se_3 FeS-FET.
Source: Adapted from Ref. [232].

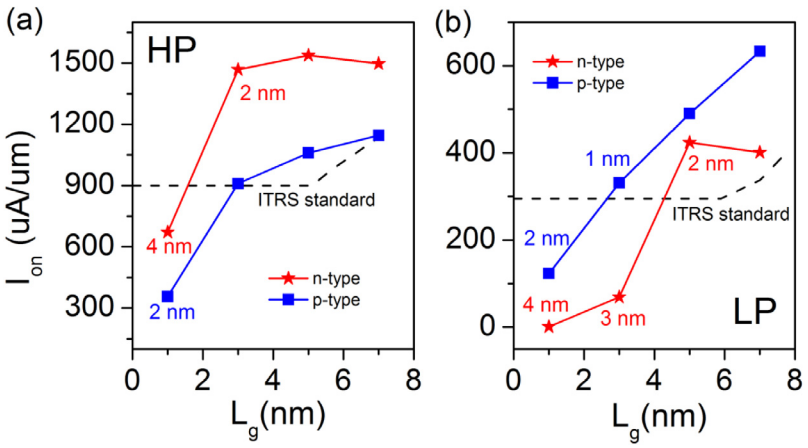


Fig. 6.3. On-state currents of the optimized *p*- and *n*-type HP (a) and LP (b) MOSFETs based on ML InSe. The UL length is marked ($L_{UL} = 0$ without mark). ITRS requirements are in black dashed lines.
Source: Adapted from Ref. [60].

7. Sub-10 nm tellurene FETs

7.1. Fundamental property of tellurene

Group VI tellurium (Te) is a member of the chalcogen element family. Bulk Te has a trigonal crystal lattice where each helical chain of Te atoms is covalently bonded together (Fig. 7.1(a–b)) [238]. 2D tellurium (tellurene) has different phases (Fig. 7.1(c–h)): α-phase tellurene, which is derived from the bulk trigonal structure, is the most stable structure for BL and FL tellurene; the tetragonal β-phase tellurene is the most stable phase for ML tellurene; γ-phase tellurene is less stable than α and β phases [239,240]. Recently, ML, BL, and FL tellurene in their most stable phase is experimentally fabricated by Huang et al. using the method of molecular beam epitaxy [241].

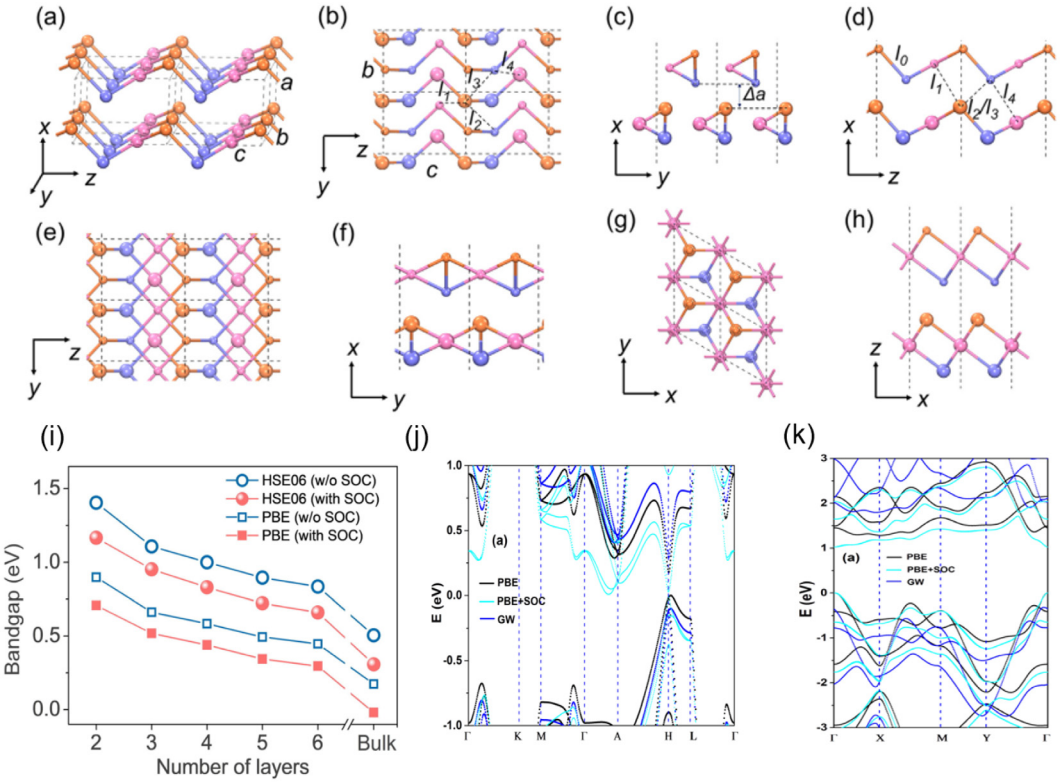


Fig. 7.1. Lattice structure and band structures of tellurium [239,243]. (a) Crystal structures of bulk Te. (b–h) Top and side view of bilayer α-Te (b–d), bilayer β-Te (e, f), and bilayer γ-Te (g, h). (i) Layer-dependent bandgaps of FL α-tellurene. (j, k) Band structures of bulk Te (j) and ML Te (β phase) (k) at PBE, PBE + SOC, and GW level.
Source: Reproduced from Ref. [239] and Ref. [243].

2D tellurene has a thickness-dependent bandgap according to the experimental measurement and the DFT calculations (Fig. 7.1(i)) [242]. The bandgap of 2D tellurene monotonically increases with the decreasing thickness from ∼0.33 eV in bulk to ∼0.92 eV in ML (β-phase) according to the scanning tunneling spectroscopy (STS) on a graphene/6H-SiC(0001) substrate [241]. Without the inclusion of spin–orbit coupling (SOC), the bandgap at the GGA level increases from ∼0.25 eV in bulk, to ∼0.85 eV in BL (α-phase) and to ∼1.45 eV in ML tellurene (β-phase), and the bandgap at GW method increases from 0.41 eV in bulk to 2.35 eV in ML (β-phase) [243]. The SOC decreases the bandgaps, and the bandgap in bulk and ML separately becomes 0.03 eV and 1.02 eV at the GGA level and becomes 0.25 eV and 1.92 eV at the GW method (Fig. 7.1(j–k)) [53,243,244]. In the following, we denote 'ML tellurene (β-phase)' as 'ML tellurene' hereafter without a particular statement. We attribute the significant bandgap discrepancy between the STS measurement and the GW method to the bandgap renormalization of ML tellurene on a metallic substrate in the STS measurement [245]. Due to the strong screening effect from the metallic substrate, the electron–electron interaction is greatly depressed, and thus the quasiparticle bandgap is reduced greatly. In such a case, the bandgap can be approximately described by the GGA, which is based on single-electron approximation.

The field-effect hole mobility of 2D tellurene increases with the thickness and peaks at ∼700 $cm^2/(V\cdot s)$ at the thickness of 16 nm at room temperature in the experiment [31,246,247]. Besides, great air stability is demonstrated for 2D tellurene for almost the entire thickness ranging from flakes to 3 nm [31]. All these merits make 2D tellurene prominent in the existing 2D semiconducting materials to construct high-speed electronics [242].

7.2. Experimental long tellurene FETs

Long-channel (300 nm∼3 μm) back-gate 2D tellurene transistors with different thicknesses have been successfully fabricated by Wang et al. [31]. Metal Pd (with a high work function) is chosen to form low-resistance *p*-type tellurene transistors [31]. As the transfer characteristics of the tellurene transistor with a thickness of 7.5 nm shows (Fig. 7.2(a)), the maximum on/off ratio is $\sim 10^5$, and the maximum drain current is 300 μA/μm [31]. The BL and ML tellurene FETs with a back gate and a long channel also have been experimentally achieved (Fig. 7.2(b–c)), and the maximum current of the BL and ML tellurene FETs is merely 10^{-1}μA/μm. The greatly degraded maximum current is blamed on the drastically reduced mobility (BL: ∼1 $cm^2/(V\cdot s)$) and a large Schottky barrier height due to the large bandgap [31].

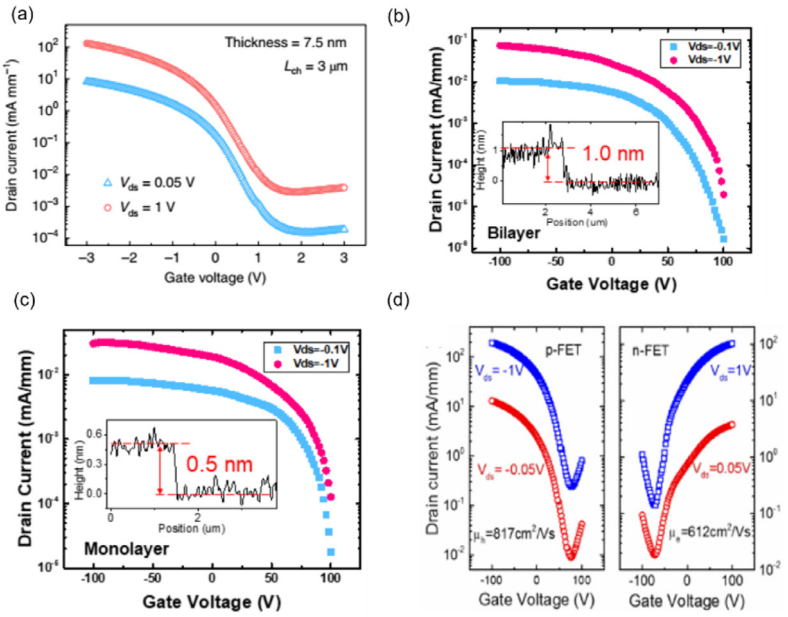


Fig. 7.2. Experimental FETs built by 2D tellurene. (a) Transfer characteristic of a long-channel tellurene transistor with a thickness of 7.5 nm and Pd electrode. Transfer curves of BL tellurene (b) and ML tellurene (c) transistors with long channels (at micron length magnitude) [31]. (d) Transfer characteristics for the few-layer tellurene FETs with $L_g = 3$ μm with Pd and Ti as the electrode, respectively [248].
Source: Reproduced from Ref. [31] and Ref. [248].

Besides, with the resort of atomic layer deposited dielectric doping technique, Qiu et al. fabricated both *p*-type and an *n*-type few-layer tellurene FETs ($L_g = 3$ μm) [248]. Their behavior is almost symmetric, with the maximum current of ∼200 μA/μm at $V_{ds} = 1$ V (Fig. 7.2(d)) [248]. Metal Ti with a low work function is used as the electrodes for the *n*-type case, and metal Pd electrode is for the *p*-type one.

7.3. Simulation of sub-10 nm ML and BL tellurene FETs

Firstly, both the simulated *p*-type DG ML and BL tellurene MOSFETs outperform their respective *n*-type counterparts in the sub-10 nm region for the HP and LP applications in terms of the *ab initio* quantum transport simulation regardless of the transport direction [53,244]. The main reason is that the electron effective mass is larger than the corresponding directional hole one (0.83 m_0 *vs.* 0.39 m_0/0.19 m_0 *vs.* 0.11 m_0/0.87 m_0 *vs.* 0.36 m_0/0.85 m_0 *vs.* 0.58 m_0 for the armchair-directed ML tellurene/zigzag-directed ML tellurene/*x*-directed BL tellurene/*y*-directed BL tellurene) [53,244]. Such a difference in the effective carrier mass leads to lower electron mobility and thus poorer *n*-type device performance.

Secondly, the sub-10 nm *p*-type ML tellurene MOSFETs outperform the *p*-type BL ones for both the HP and LP applications, regardless of the transport direction. For example, the *p*-type ML tellurene MOSFETs meet the I_{on} HP and LP requirements of the ITRS until L_g is scaled down to 4 (zigzag-directed) and 5 nm (armchair-directed), respectively (Fig. 7.3(a)) [244]. By contrast, both the *x*- and *y*-directed *p*-type BL ones at $L_g = 5$ ∼9 nm only satisfy 82%∼95% of the I_{on} HP standards of the ITRS, and I_{on} for the LP applications is even unavailable due to the large leakage currents [53]. Consistently, the *p*-type 5 nm-L_g ML tellurene MOSFETs generally show a smaller *SS*, faster-switching speed, and less energy consumption than the BL counterparts, regardless of the transport direction (Fig. 7.3(b–d)) [53,244]. Such better performance for the *p*-type ML tellurene devices is attributed to its thinner channel and thus a shorter characteristic length λ (0.89 nm at $L_g = 1$ ∼5 nm for ML tellurene *vs.* 1.26∼1.44 nm at $L_g = 5$ ∼9 nm for BL tellurene) [53,244].

Thirdly, the *p*-type armchair-directed (*y*-directed) ML (BL) tellurene MOSFETs have a smaller *SS* at a given L_g and thus a better gate control than the zigzag-directed (*x*-directed) counterparts in the subthreshold region (Fig. 7.3(b)). The reason is that the effective hole mass of the armchair-directed (*y*-directed) ML (BL) tellurene is larger than that of the zigzag-directed (*x*-directed) counterparts [53,244]. Such a difference in effective hole mass leads to suppression of the direct tunneling leakage from the source to drain. Most of the studied *p*-type ML ($L_g = 1$ ∼5 nm) and BL ($L_g = 5$ ∼9 nm) tellurene MOSFETs can well or nearly meet the τ and PDP requirements of the ITRS for the HP and LP applications (Fig. 7.3(c, d)).

Both the ML and BL tellurene channels always form lateral Schottky contacts with common bulk metal electrodes (Sc, Ag, Cu, Au, Ni, Pt, *etc.*) in terms of the *ab initio* quantum transport simulation, regardless of the transport direction, due to the strong Fermi level pinning [250,251]. Fortunately, ML tellurene could form a lateral *p*-type Ohmic contact with the

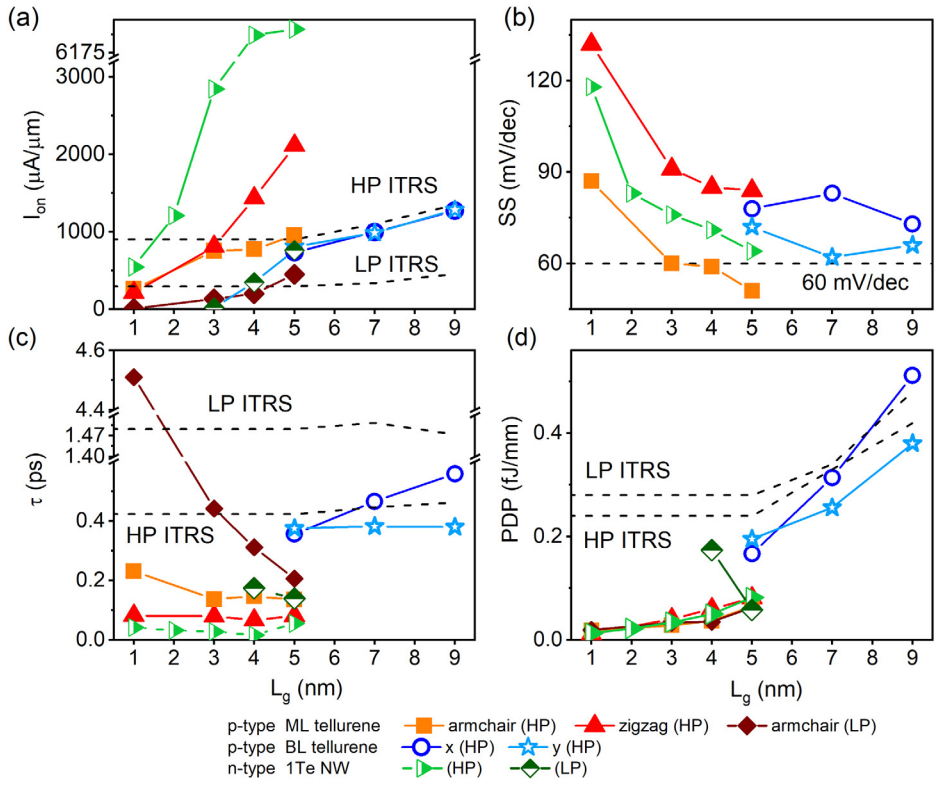


Fig. 7.3. UL-optimized (a) on-state current, (b) subthreshold swing, (c) delay time, and (d) power-delay product of the sub-10 nm *p*-type ML and BL tellurene MOSFETs and *n*-type 1Te NW GAA MOSFETs as a function of the gate length.
Source: Reproduced from Ref. [244], Ref. [53] and Ref. [249].

graphene electrode along with the armchair and zigzag directions [250]. Besides, a lateral quasi-Ohmic contact with a hole SBH of 0.08 eV is formed in the *x*-directed BL tellurene channel contacted with graphene electrodes [251]. Therefore, graphene is probably the optimal electrode material for the ML and BL tellurene transistors.

Recently, freestanding Te nanowires (NWs) have been successfully fabricated by a substrate-free solution process [252]. The bare Te NWs with a diameter of 25 nm show good carrier mobility of more than 600 $cm^2/V{\cdot}s$ [252]. The fabricated *p*-type FETs based on the 13 nm-diameter bare Te NWs with $L_{ch} = 1$ μm possess a high current on/off ratio of 10^4 at $V_d = 0.05$ V and maximum current of 700 μA/μm at $V_g = -40$ V [252] (Fig. 7.4(a)). The diameter of the bare Te NWs in FETs is limited to 6 nm, and using boron nitride nanotubes (BNNTs) encapsulation can break this limitation [252]. The 2 nm-diameter Te NWs *n*-type FETs encapsulated in BNNTs with $L_{ch} = 100$ nm have been fabricated with a current on/off ratio on the order of $\sim 10^2$ [252] (Fig. 7.4(b)).

The *n*- and *p*-type sub-5 nm GAA single-Te-chain NW (1Te) and three-Te-chain NWs (3Te) MOSFETs have been simulated based on the *ab initio* quantum-transport methods. The *n*-type sub-5 nm GAA 1Te MOSFETs are predicted to have the most outstanding transport performance among the *n*- and *p*-type 1Te and 3Te GAA MOSFETs for both the HP and LP applications [249]. The main reason is that the *n*-type 1Te devices possess the smallest effective carrier mass among the *n*- and *p*-type 1Te and 3Te ones (0.30 m_0 for 1Te electron, 1.17 m_0 for 1Te hole, 0.69 m_0 for 3Te electron, 0.35 m_0 for 3Te hole) [249], and a shorter λ than the 3Te ones (1Te: 0.63 nm *vs.* 3Te: 0.89 nm).

The sub-5 nm GAA 1Te MOSFETs have comparable channel thickness with the DG ML tellurene MOSFETs. Owing to the shorter λ (1Te: 0.63 nm *vs.* ML tellurene: 0.89 nm) and comparable effective carrier mass (0.30 m_0 for 1Te electron *vs.* 0.11 ∼ 0.87m_0 for ML tellurene electron and hole), the *n*-type sub-5 nm GAA 1Te devices outperform both the *n*- and *p*-type DG ML tellurene counterparts for the HP and LP applications, regardless of the transport direction (Fig. 7.3). By contrast, the *p*-type 1Te ones perform worse than the latter due to the much larger effective carrier mass (1.17 m_0 for 1Te hole) and thus lower hole mobility [244,249]. Anyway, the 1D Te NWs GAA MOSFETs could have comparable transport performance with the 2D tellurene DG ones when they have comparable channel thickness.

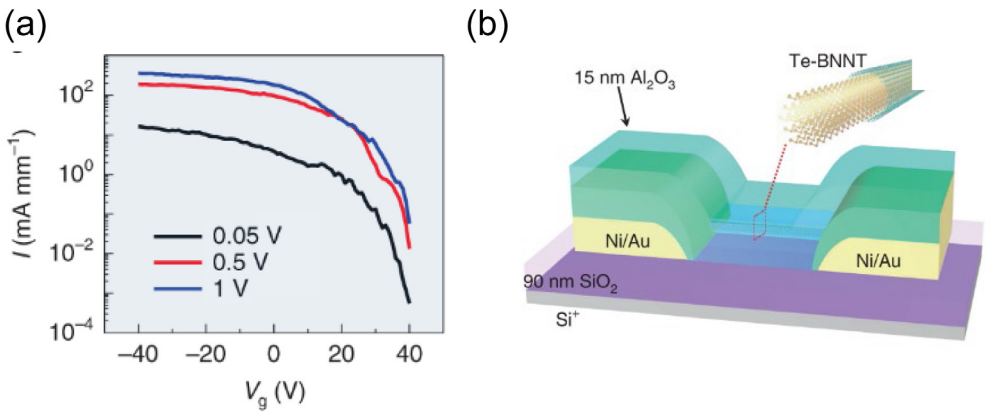


Fig. 7.4. (a) Transfer characteristics of a *p*-type 13 nm-diameter Te NWs FET contacted with Ni/Au electrodes. (b) Schematic of the Te NWs FETs encapsulated by boron nitride nanotubes.
Source: Reproduced from Ref. [252].

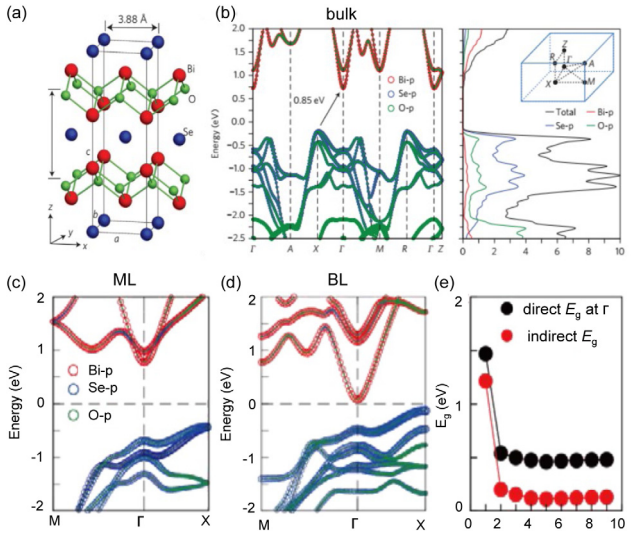


Fig. 8.1. (a) Lattice structure of Bi_2O_2Se. (b) DFT-calculated band structure and density of states of bulk Bi_2O_2Se with optimization of LDA-MBJ and spin–orbital coupling. (c, d) DFT-calculated band structures of ML and BL Bi_2O_2Se. (e) Bandgap E_g evolution as the function of the thickness.
Source: Reproduced from Ref. [26].

8. Sub-10 nm Bi_2O_2Se FETs

8.1. Fundamental properties of Bi_2O_2Se

Bi_2O_2Se, as a traditional thermoelectric material, exhibits a layered structure, in which Se^- sandwiches the $[Bi_2O_2]^{2+}$ layers under weak electrostatic interaction, as shown in Fig. 8.1(a) [26,253–255]. H. Boller first synthesized it at high temperatures in 1973 [256]. Recently, 2D Bi_2O_2Se down to BL and ML is successfully fabricated on mica substrate via chemical vapor deposition (CVD) by Peng et al. [26,257]. 2D Bi_2O_2Se shows robust ambient and thermal stability. The electron Hall mobility of 2D Bi_2O_2Se is 450 $cm^2/V{\cdot}s$ at room temperature and 29000 $cm^2/V{\cdot}s$ at 1.9 K [26,253,257]. The bandgap of Bi_2O_2Se is thickness-dependent, and those of the ML and BL Bi_2O_2Se are 1.14 eV and 0.18 eV, respectively, at the local density approximation-modified Becke-Johnson (LDA-MBJ) and spin–orbit coupling level.

8.2. Experimental long 2D Bi_2O_2Se FETs

Since the fabricated large-area thin Bi_2O_2Se crystal has a light effective mass ($m^* = 0.14 \pm 0.02 m_0$) and large bandgap (0.85 eV), it is a promising candidate for high-performance electronic devices. The top-gated Bi_2O_2Se FET with a channel thickness of 6.2 nm and a channel length of 21 μm has been successfully fabricated (Fig. 8.2(a)) [26]. An Ohmic contact

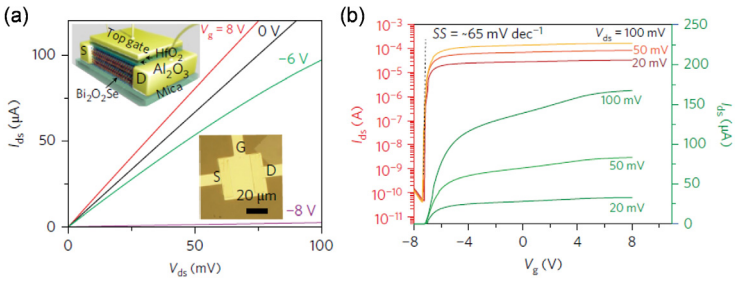


Fig. 8.2. 2D Bi_2O_2Se FET. (a) Output curves. The insets are a schematic device model of a top-gated Bi_2O_2Se transistor and an optical microscopy image of this device on mica substrate with Al_2O_3 and HfO_2 as the dielectrics. (b) Transfer characteristics at different biases. The transistor is 6.2 nm-thick and 21 μm-long. Pd/Au metal electrodes are used.
Source: Reproduced from Ref. [26].

is achieved using Pd/Au metal as electrodes. A large on/off current ratio (> 10^6) and an ideal *SS* value (65 mV/dec) are achieved (Fig. 8.2(b)). The BL Bi_2O_2Se FET with a top gate has also been experimentally designed. Like the FL counterpart, the linear output curve indicates Ohmic contact, and the transfer characteristic shows a maximum on/off ratio of 10^6 for electron accumulation [26]. All the device performances are observed at room temperature.

8.3. Simulation of sub-10 nm ML and BL Bi_2O_2Se FETs

The optimized *p*- and *n*-type ML Bi_2O_2Se transistors are predicted to reach the ITRS HP goals for the on-state current until L_g is shortened to 2 and 3 nm, respectively [73]. The corresponding delay time and PDP are also small enough to meet the goals (Fig. 8.3). Significantly, the 9 nm-L_g ML *n*-MOSFET demonstrates a remarkably high on-state current of more than 3000 μA/μm. By contrast, the BL counterparts pale [101]. The on-state current shows a more than 50% decrease when the channel changes from ML to BL at a given L_g. The *n*-type sub-10 nm BL Bi_2O_2Se transistors reach the ITRS HP goals for the on-state current until 5 nm, while all the studied *p*-type ones fail to meet the goals. Partly due to the smaller on-state current, the delay time of the BL ones are generally larger than the corresponding ML ones for either the *n*-type or *p*-type at a given L_g. PDP of the ML and BL Bi_2O_2Se transistors keep at a similar level.

Two factors contribute to the poorer performance of the BL Bi_2O_2Se transistors than the ML ones. One is the degradation of the gate control ability with the increasing layer number, and the other one is the increase of the leakage current due to the much smaller bandgap (ML: 1.14 eV versus BL: 0.18 eV at the GGA level), making it hard to turn "off". As the layer number increases in 2D Bi_2O_2Se, the thickness keeps increasing, and the bandgap keeps decreasing. Therefore, it is expected that the device performance of the multi-layer Bi_2O_2Se FETs would not exceed that of the ML ones. 2D Bi_2O_2Se FETs in the sub-10 regime are less satisfying for the LP applications. The leading cause is the sizeable off-state current due to the small effective mass (0.12–0.19 m_0). This fact is contrast with the case of 2D MoS_2, which is predicted to be suitable for LP but not HP applications due to the large effective mass and low carrier mobility.

In practice, the contact is of great importance in the 2D FET with a very short channel length. Pt, Sc, or Ti electrodes are suggested to be used as electrodes for the transistors with ML Bi_2O_2Se channels [258], and Au, Pd, Pt, Ti, or Sc electrodes are suggested for the one with BL Bi_2O_2Se in view of the formation of the *n*-type Ohmic contacts [259]. Given these metals as electrodes, the sub-10 nm ML and BL Bi_2O_2Se SBFETs are likely to approach the theoretical performance limit of the corresponding MOSFET counterparts. Other bismuth oxychalcogenide members (Bi_2O_2S and Bi_2O_2Te) [260–262] share similar physical nature with Bi_2O_2Se, including bandgap and effective mass. Therefore, the device performance based on these materials is worthy of being investigated.

In 1984, Koyama et al. synthesized the bulk Bi_2O_2S for the first time [263]. Recently, 2D Bi_2O_2S nanosheets with the thickness down to 2–3 nm have been successfully synthesized via a one-pot wet-chemical synthetic method by Yan et al. [264]. 2D Bi_2O_2S nanosheets have a bandgap of around 1.5 eV, and they are demonstrated to be stable in the air. Xu et al. have calculated the intrinsic properties of the ML fully hydrogen-passivated $Bi_2O_2S_2$ ($Bi_2O_2S_2H_2$) based on the first-principles simulation [265]. The calculated bandgap of the ML $Bi_2O_2S_2H_2$ is 1.92 eV at the DFT-GGA level. According to the deformation potential theory, the ML $Bi_2O_2S_2H_2$ possesses an ultrahigh electron mobility of 16.4 × 10^3–26.7 × 10^3 cm^2/V·s and a moderate hole mobility of 0.264 × 10^3–0.968 × 10^3 cm^2/V·s at 300 K. Besides, the simulated maximum/minimum current ratio of the ML $Bi_2O_2S_2H_2$ FET with Ti electrode at L_g = 5 nm reaches 10^5 by using the *ab initio* quantum transport simulation.

Bi_2OS_2 is another kind of bismuth oxysulfide. The bulk Bi_2OS_2 has a vdW layered structure, and every single layer of the Bi_2OS_2 has a triple-layer structure with a $[Bi_2O_2]^{2+}$ layer sandwiched between two $[BiS_2]^-$ layers. Bulk Bi_2OS_2 is firstly reported by Tyrel et al. in 2013 [266]. Very recently, Yu et al. have successfully synthesized 2D Bi_2OS_2 with a thickness of about 0.8–1.0 nm by hydrothermal method and ultrasonication process [267]. Experimentally, bulk Bi_2OS_2 has a measured optical gap of 0.99 eV [268]. The first-principles calculation performed by Wang et al. shows that the Bi_2OS_2 possesses a layer-dependent bandgap at the DFT-GGA level [269]. The calculated bandgap of Bi_2OS_2 firstly declines from 0.92 eV

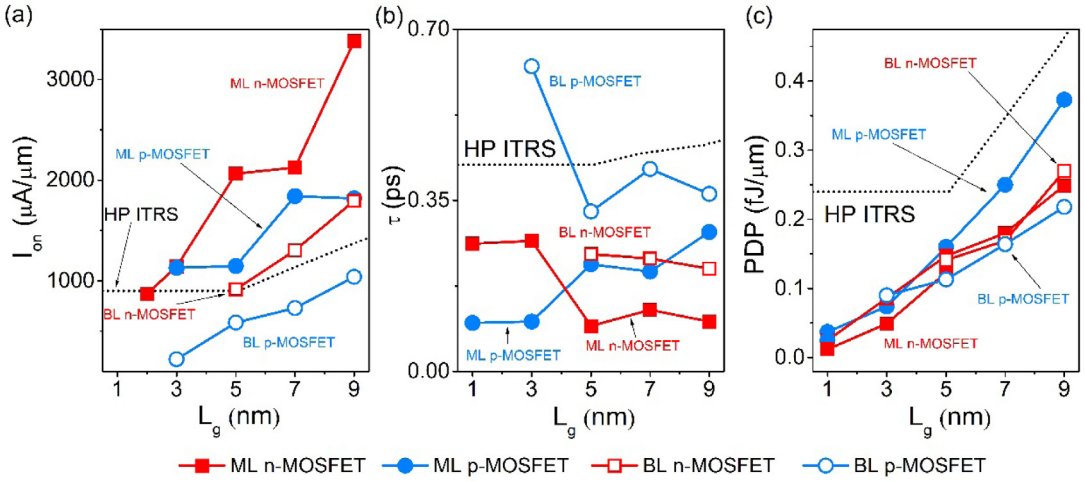


Fig. 8.3. (a) On-state current, (b) intrinsic delay time, and (c) PDP of the simulated sub-10 nm ML and BL Bi_2O_2Se MOSFETs as a function of the gate length.
Source: Reproduced from Refs. [73,101].

(bulk) to the minimum value of 0.59 eV (8-layer) and then gradually increases to 0.97 eV (ML). Based on the deformation potential theory, 2D Bi_2OS_2 possesses an ultrahigh electron mobility with the value increasing from 6.67 × 10^3 cm^2/V·s (ML) to 26.6 × 10^3 cm^2/V·s (trilayer) and a moderate hole mobility with the value increasing from 0.49 × 10^3 cm^2/V·s (ML) to 0.73 × 10^3 cm^2/V·s (trilayer) at 300 K. These properties render 2D Bi_2OS_2 a promising channel candidate for the high-performance sub-10 nm FETs.

9. Sub-10 nm 2D TFETs

9.1. Mechanism and advantage of 2D TFETs

A TFET is usually actualized with a p-i-n structure, as displayed in Fig. 9.1(a) [9], and the primary injection mechanism is the so-called band-to-band tunneling. Through controlling the band bending of the channel by changing the gate voltage, the TFET can be switched between on- and off-state (see Fig. 9.1(b)) [9]. At the off-state, a wide tunneling barrier is formed. At the on-state, the tunneling barrier width is greatly reduced because the channel valence band moves above the source conduction band by the gate voltage (*p*-type case).

In a normal FET like MOSFET, the charge carrier transports over a barrier by thermal injecting so that the Boltzmann tail of a semiconductor band (see Fig. 9.1(c)) [270] would lead to the so-called Boltzmann thermionic limit of *SS* (60 mV/dec). This limit is the obstacle for degrading a device's energy consumption because of the nonreducible leakage current and supply voltage brought by the Boltzmann tail raised from the thermal transport mechanism itself. While in a TFET, the source carriers in the Boltzmann tail cannot tunnel to the drain because no empty states are available in the channel bandgap, so a sharp slope of less than 60 mV/dec is achieved, as shown in Fig. 9.1(d) [270]. The reduced *SS* would reduce the V_{dd} while maintaining the same on/off ratio.

However, a very low current is usually obtained with a conventional bulk channel despite the very steep *SS*, which is the main block of the TFET application. Using a 2DSC channel is a possible way to promote the current. The atomic-thin body guarantees good gate control ability, the flat surface suppresses the carrier scattering, the absence of the dangling bond reduces the unwanted states in the tunneling region [271], and vdW stacking of the *p*- and *n*-type 2DSC has a very thin tunneling region [9] (termed thin tunneling FET (thinTFET)), allowing a large tunneling current.

Energy-delay product (EDP) is the combined metric to characterize the trade-off between energy consumption and delay time. An HP CMOS is the core of a chip of a server and runs fast but consumes more energy. By contrast, an LP CMOS is the core of a chip of a smartphone and tablet and runs slowly but consumes less energy. An ideal FET should operate very fast with less energy consumption. A key challenge of the semiconductor device design is to fabricate a device close to the preferred corner of the EDP (Fig. 9.2). A simulation has shown that the thinTFET and TMD TFET have exhibited an advantage over the CMOS HP and LP devices in terms of the EDP [264,272].

9.2. Experimental long 2D TFETs

An atomic heterojunction (HetJ) thinTFET is fabricated at a several-micrometer scale using a highly doped *p*-type germanium (Ge) and a $BLMoS_2$ as source and channel, respectively (see the schematic view in Fig. 9.3(a)) [273]. This

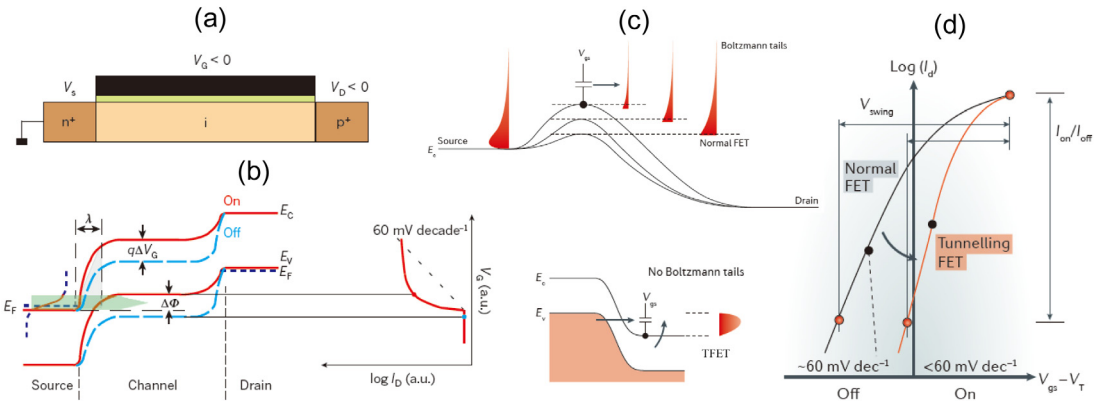


Fig. 9.1. (a) Schematic view and (b) energy band profile for off- and on-states and transfer characteristic of a *p*-type TFET. (c) Compared effects of Boltzmann tails and (d) transfer characteristics in a normal FET and a TFET.
Source: Reproduced from Refs. [9,270].

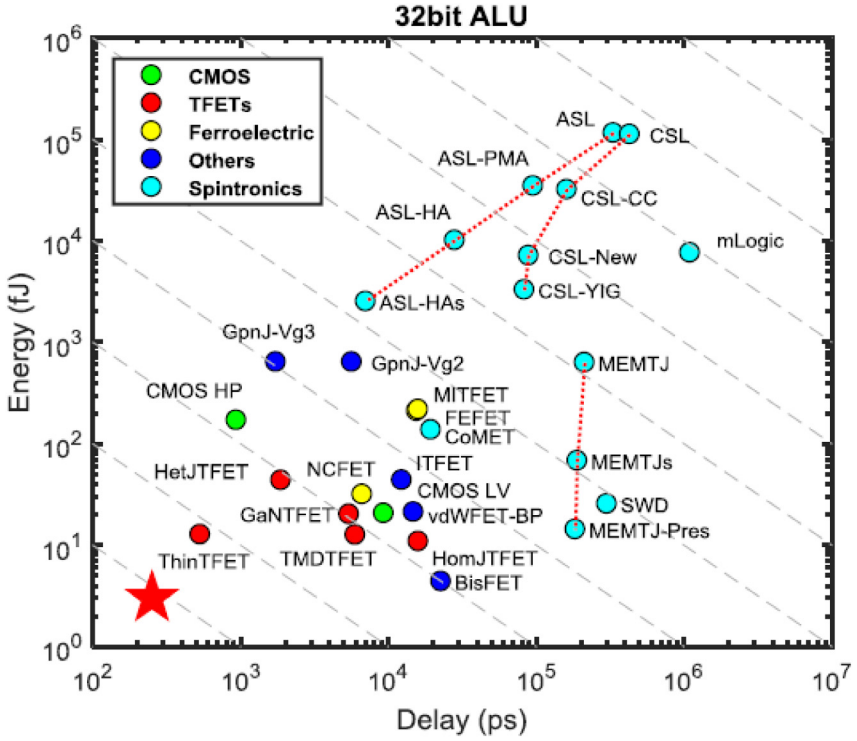


Fig. 9.2. Energy versus delay of a 32 bit arithmetic logic unit (ALU) for a variety of devices.
Source: Reproduced from Ref. [272].

vertical 3D Ge/2D MoS_2 HetJ TFET has an excellent electrostatic, a less-strained interface, a low tunneling barrier, and a large overlapping area. The device is measured in a three-terminal configuration (Fig. 9.3(b)), and the transfer characteristics with varying V_D are given in Fig. 9.3(c). The 3D Ge/2D MoS_2 HetJ thinTFET can overcome the Boltzmann limit on *SS* in a MOSFET over about four decades of I_D for all three V_D. *SS* of the HetJ thinTFET compared with a conventional MOSFET is given in Fig. 9.3 (d), where the MoS_2 thickness and the measure condition are the same for the TFET and MOSFET. The minimum *SS* is 3.9 mV/dec, and the average *SS* is 31.1 mV/dec over more than four decades of drain currents for the TFET, while the lowest *SS* achieved for the MOSFET is 60 mV/dec.

Besides the vertical 3D Ge/2D MoS_2 HetJ thinTFET, interlayer tunneling currents have also been detected in the vertical MoS_2/WSe_2, $WSe_2/SnSe_2$, and MoS_2/BP based devices (micrometer scale) through vdW stacking, as shown in Fig. 9.4. A large reverse bias tunneling current is obtained like a diode when the vertical MoS_2/WSe_2 HetJ device [274] is backward gate modulated. In the vertical $WSe_2/SnSe_2$ HetJ thinTFET [276], the minimum *SS* is 37 mV/dec, and the average *SS* is 80

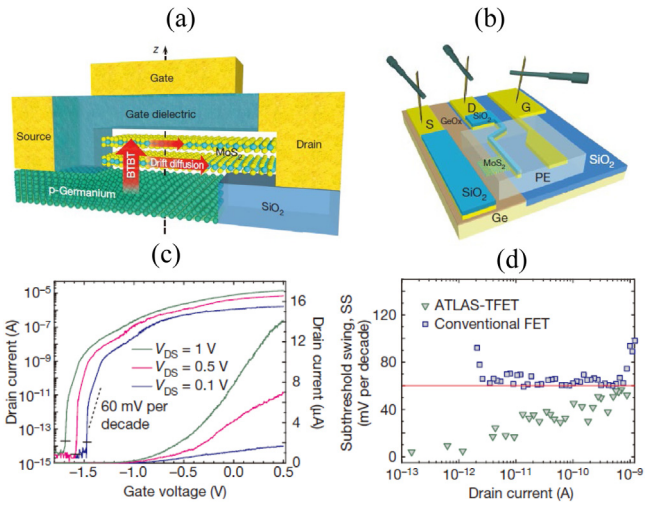


Fig. 9.3. (a) Vertical 3D Ge/2D MoS_2 HetJ thinTFET model. (b) Schematic view of the characteristic measurement of the TFET. Here, the device length is 5.1 μm, width 15 μm, and the overlap area of MoS_2 and Ge 54.6 μm^2. (c) I_D–V_G curves with varying V_D. (d) *SS* as a function of I_D for the vertical 3D Ge/2D MoS_2 HetJ TFET compared with a conventional MOSFET.
Source: Reproduced from Ref. [273].

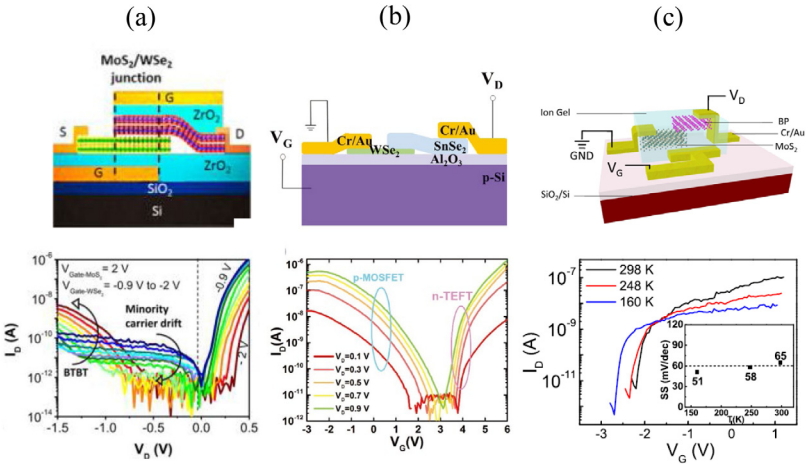


Fig. 9.4. (a) Schematic view and I_D–V_D curves with varying V_{G-WSe_2} (V_{G-MoS_2} = 2 V) of the dual-gated vertical MoS_2/WSe_2 HetJ TFET. (b) Schematic view and I_D–V_G with varying V_D of the vertical WSe_2/$SnSe_2$ HetJ TFET. (c) Schematic view and I_D–V_G of the vertical MoS_2/BP HetJ thinTFET with the corresponding minimum *SS* in the inset.
Source: Reproduced from Ref. [274] , Ref. [275] and Ref. [276].

mV/dec for exceeding two decades of I_D at room temperature with a positive back-gate voltage. In the vertical MoS_2/BP HetJ thinTFET [275], the obtained *SS* is 65 and 51 mV/dec at 300 and 160 K, respectively, and the low *SS* values can maintain over two decades of I_D.

In the above HetJ thinTFETs, the *SS* over four decades of I_D (SS_{ave_4dec}) can maintain sub-thermionic value (*i.e.*, sub-60 mV/dec) only in the 3D Ge/2D MoS_2 HetJ thinTFET, but the I_{60} (I_D where *SS* becomes 60 mV/dec) is still very low (4.2×10^{-5} μA/μm, see Fig. 9.3(d)). Thus, I_{on} of the above HetJ thinTFETs is too low for practical application. The low I_{on} may come from two reasons: (1) the intrinsic electronic properties of TMDCs like large effective masses; (2) the interface problems like defects, oxides, and lattice mismatches. Very recently, a thickness-controlled BP natural HetJ TFET has been fabricated with the small-bandgap bulk BP as the source and large-bandgap ML BP as a channel (natural heterojunction TFET (NHetJ TFET), see Fig. 9.5(a)) [277]. At on-state of such an NHetJ TFET, the tunneling barrier height is determined by the bandgap of bulk BP (0.3 eV), and the on-state current is maximized. While at the off-state, the tunneling barrier height is determined by the bandgap of ML BP (1.0 eV), and the off-state current is minimized (Fig. 9.5(b)). By taking advantage of different tunneling barrier heights, very steep *SS* is available from both the *p*- and *n*-type transfer curves in Fig. 9.5(b), and SS_{ave_4dec} values of the *p*- and *n*-type BP NHetJ TFETs are only 23.7 and 24.0 mV/dec, respectively. The performance of the BP NHetJ TFETs is compared with those of the two known sub-thermionic HetJ TFETs (*i.e.*, the Si/III–V

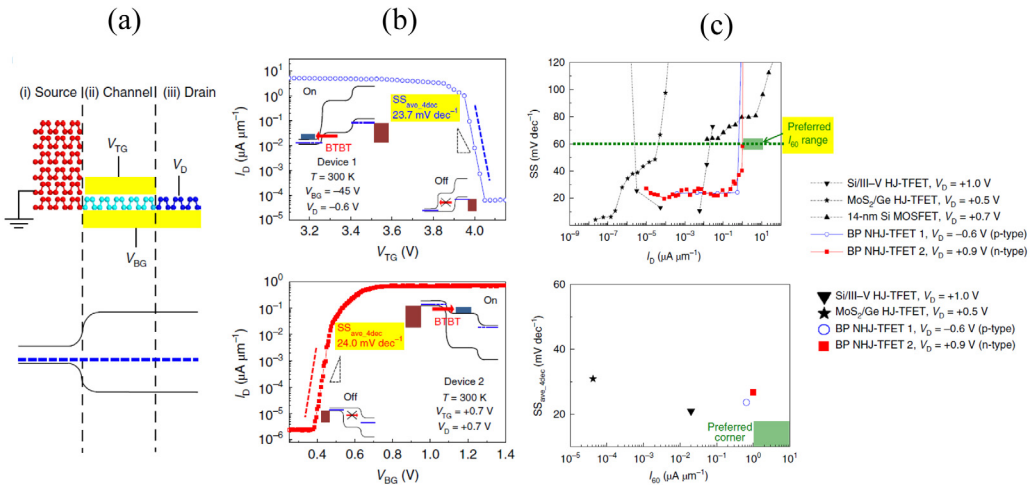


Fig. 9.5. (a) BP band properties and (b) transfer characteristic for the *p*- and *n*-type BP NHetJ TFETs at $|V_D| \leq 0.7$ V. (c) Comparison of *SS* (*vs.* I_D) and SS_{ave_4dec} (*vs.* I_{60}) of the BP NHetJ TFETs with the two recent reported sub-thermionic HetJ TFETs and a 14 nm Si MOSFET.
Source: Reproduced from Ref. [277].

Table 9.1
Comparison of the device performances of the ML BP, GeSe, and WTe_2 HomJ TFETs between the *ab initio* level and tight-binding (TB) level. The device setting parameters are similar for the two methods.

	L_g(nm)	I_{max} (μA/μm)	I_{on} (μA/μm)	τ (ps)	PDP (fJ/μm)
BP (*ab initio*) [282]	10	3.5×10^3	–	–	–
BP (TB) [279]	10	2×10^2	–	–	–
GeSe (*ab initio*) [283]	10	–	85	0.332	0.014
GeSe (TB) [278]	10	–	6.09	3.05	0.009
WTe_2 (*ab initio*)	10	–	30.2	1.52	0.081
WTe_2 (TB) [280]	15	–	350	0.135	0.067

and 3D Ge/2D MoS_2) in Fig. 9.5(c). I_D at the sub-thermionic *SS* is significantly higher in the BP NHetJ TFETs, and I_{60} of 0.65∼1 μA/μm is about two orders of magnitude larger than that of the Si/III–V HetJ TFET and more than four orders of magnitude larger than that of the 3D Ge/2D MoS_2 HetJ thinTFET.

9.3. Simulation of sub-10 nm 2D TFETs

9.3.1. Comparison between the ab initio method and semi-empirical method

Many former simulations on 2D TFETs are based on the semi-empirical tight-binding approximation [278–281], where the parameterization of the transition matrix may introduce a large error because the transition matrix is not transferable. A benchmark of the device performances of the ML BP, GeSe, and WTe_2 planar homojunction (HomJ) TFETs at the *ab initio* level against those at the TB level under similar conditions (L_g, EOT, N_S/N_D, V_{dd}, *etc.*) is given in Table 9.1 [282,283]. A significant discrepancy of up to one order of magnitude (either smaller or larger) on the on-state current and delay time is found between the two methods despite a similar PDP. For example, I_{on}, τ, and PDP of the ML GeSe HomJ TFET are 85 μA/μm, 0.332 ps, and 0.014 fJ/μm at the *ab initio* level, compared with 6.09 μA/μm, 3.05 ps, and 0.009 fJ/μm at the TB level. Thus, to perform an *ab initio* quantum transport simulation is necessary to predict the TFET device on-state current and speed accurately.

9.3.2. 2D group V TFETs

The device model of the sub-10 nm ML BP HomJ TFET that transports along the armchair direction is given in Fig. 9.6(a). The benchmark of I_{on} of the optimal ML BP TFETs at L_g = 1–10 nm against the MX_2 TFETs and ITRS HP target is provided in Fig. 9.6(b) [282,284]. I_{leak} of the ML BP TFET exceeds the I_{off} request of the LP device, rendering ML BP TFET unsuitable for the LP device. I_{on} of the optimal ML BP HomJ TFETs monotonously increases with the increasing L_g and meets the ITRS HP goal at L_g = 4–10 nm. I_{on} of the ML BP HomJ TFET is higher than those of the examined ML MX_2 counterpart except for the WTe_2 HomJ TFET at L_g = 7 nm. The minimum *SS* of the sub-10 nm ML BP HomJ TFETs is given in Fig. 9.6(c). *SS* monotonously decreases with the increasing L_g, and sub-60 mV/dec of *SS* are acquired at L_g = 9–10 nm. With similar L_g, these *SS* values are much smaller than both their SBFET and MOSFET counterparts.

The HomJ thinTFET model with the vertical stacked ML BP along the armchair direction is given in Fig. 9.7(a), where the optimal overlapped region is 1 nm [283]. The vertical BP thinTFETs can serve as not only the HP device but also the LP

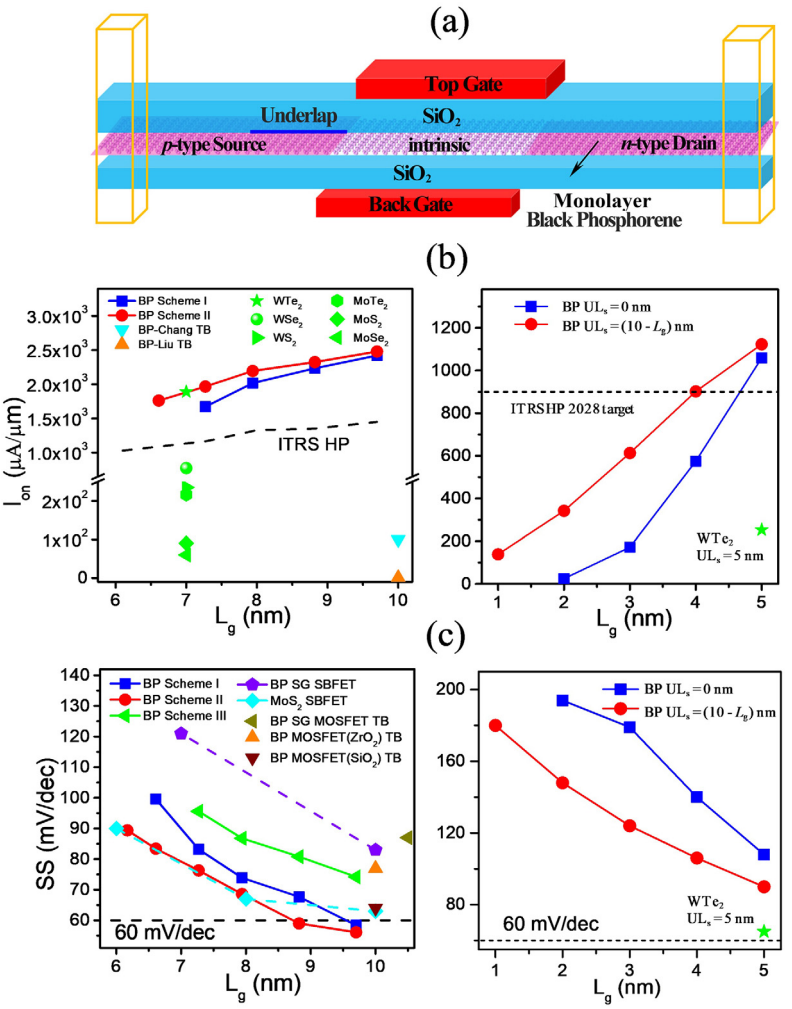


Fig. 9.6. (a) ML BP double-gated (DG) planar HomJ TFET model. (b–c) Benchmark of I_{on} (b) and minimum *SS* (c) of the optimal sub-10 nm ML BP TFETs as a function of L_g against the ML MX_2 TFET and ITRS HP device target (2013 version).
Source: Reproduced from Ref. [282] and Ref. [284].

device at the sub-10 nm scales, and a comparison of I_{on} (LP) and I_{on} (HP) with other 2D devices is provided in Fig. 9.7(b–c). The I_{on} (LP) values of the vertical BP thinTFETs touch the ITRS LP target till $L_g = 5$ nm and outperform the MoS_2 SBFET. The I_{on} (HP) values of the vertical BP thinTFETs touch the ITRS HP target until $L_g = 3$ nm and outperform the planar BP counterpart at $L_g = 1$–5 nm but is inferior to the latter at larger L_g. From Fig. 9.7(d), smaller *SS* is obtained in the vertical BP thinTFETs than their planer counterparts.

The subthreshold gate control of the vertical BP thinTFETs is better than their planar BP counterparts. The junction length (or the tunneling barrier width) is the interlayer distance, quite small (0.4 nm) in the vertically stacked TFET configuration compared with that (5 nm) in the planar TFET configuration. Such a thin tunneling barrier width is in favor of tunneling and leads to improved gate electrostatics.

9.3.3. 2D group IV mono-chalcogenide TFETs

The ML group-IV mono-chalcogenide planar HomJ TFETs [265,283] have anisotropic transfer characters, and I_{on} along the zigzag direction are higher than those along the armchair direction. In the following, the transport direction is the optimal direction for all the TFETs. Especially, I_{on} (HP) of the ML GeSe, SnSe, and GeTe planar TFETs fulfill the ITRS HP device target. I_{on} of the optimal ML GeSe planar TFET outperforms the ITRS LP devices (461 μA/μm), which is the only reported 2D TFETs in the homogeneous planar architecture to surpass the ITRS LP I_{on} target at the *ab initio* level. A faster switching speed is found in the ML GeSe, SnSe, and GeTe planar TFETs, and the low energy consumption is found for all the ML group-IV mono-chalcogenide TFETs, where τ and PDP are only one-tenth of the ITRS HP/LP required values.

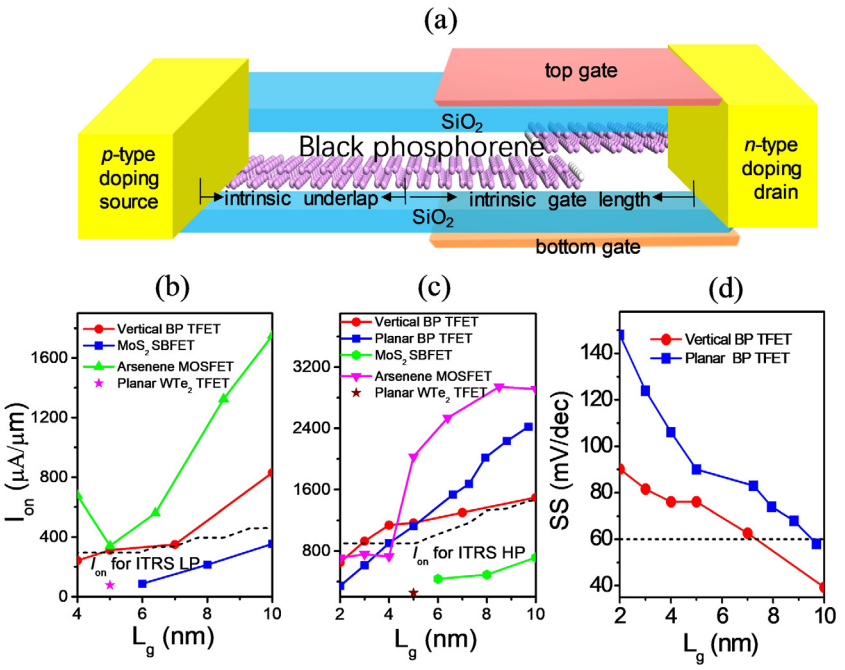


Fig. 9.7. (a) Device model of the vertical BP thinTFET. (b–d) Scaling behavior of I_{on} (LP), I_{on} (HP), and minimum *SS* of the sub-10 nm vertical BP TFETs and benchmark against other 2D planar HomJ TFETs and ITRS standards.
Source: Reproduced from Ref. [283].

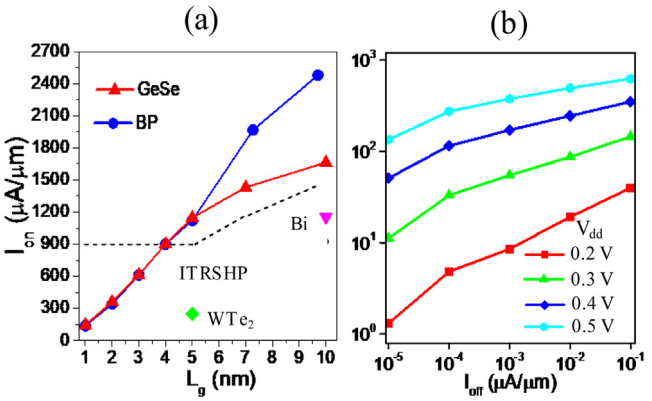


Fig. 9.8. (a) Scaling behavior of I_{on} (HP) of the sub-10 nm ML GeSe planar HomJ TFETs and comparison with other 2D ML planar HomJ TFETs and ITRS standard. (b) I_{on} of the ML GeSe planar TFET ($L_g = 10$ nm) as a function of I_{off} at a lower supply voltage of $V_{dd} = 0.2$–0.5 V.
Source: Reproduced from Ref. [283].

The scaling limit of the optimal ML GeSe planar HomJ TFET with L_g and V_{dd} is checked [283]. When scaling down with L_g, I_{leak} increases and fails to meet the ITRS LP request. In Fig. 9.8(a), I_{on} (HP) of the ML GeSe planar TFETs decreases as L_g decreases and surpasses the ITRS HP devices till $L_g = 4$ nm.I_{on}(HP) of the ML GeSe planar TFETs is smaller than the ML BP planar TFETs at a longer L_g (7–10 nm), and it becomes nearly equal to the ML BP planar TFETs at a shorter L_g (sub-5 nm) and surpasses the ML bismuthene and WTe_2 planar TFETs at $L_g = 10$ nm. In Fig. 9.8(b), I_{on} *vs.* I_{off} of the optimal ML GeSe planar TFET at $V_{dd} = 0.2$~0.5 V is given ($L_g = 10$ nm). I_{on} rapidly descends as V_{dd} decreases at the same I_{off}.

In order to decrease the leakage current, Liang et al. investigated a vertical HomJ thinTFET by stacking two SnSe layers similar to the vertical BP HomJ TFET in Fig. 9.7(a). The vertical stacked SnSe HomJ thinTFET [285] can serve as an LP device at the sub-10 nm scales compared with the planar counterpart, which is used as an HP device. With the decreasing L_g, I_{on} decreases, τ increases obviously, but PDP is almost unchanged. I_{on} touches the ITRS LP targets at $L_g = 10$ nm, but τ and PDP fulfill the ITRS LP required values at smaller $L_g = 5$–10 nm (See Fig. 9.9).

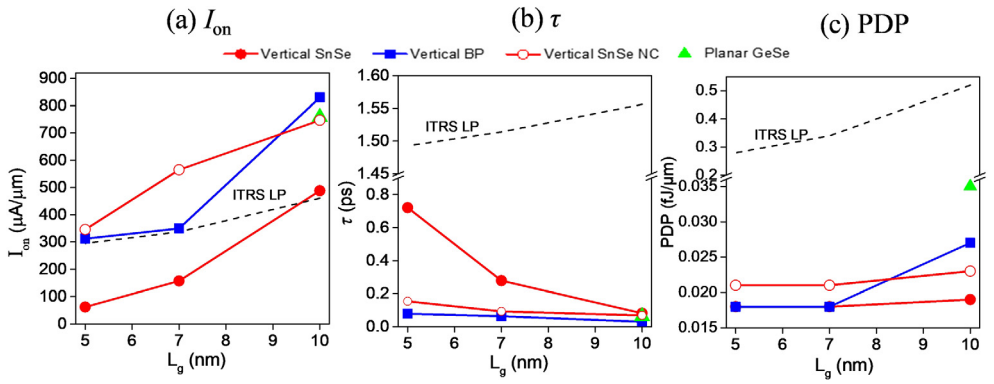


Fig. 9.9. (a) I_{on}, (b) τ, and (c) PDP as a function of L_g of the optimal sub-10 nm vertical SnSe HomJ *p*-TFETs and *p*-NCTFETs (V_{dd} = 0.64–0.74 V) and comparison with those of planar GeSe HomJ TFET, vertical BP HomJ TFETs, and the ITRS requirements for the LP devices.
Source: Reproduced from Ref. [285].

Since the layer-controlled bandgap of a 2D material could improve I_{on} of a TFET, the BL-ML SnS NHetJ TFET is built with BL SnS as the source and ML SnS as the channel and drain, as shown in Fig. 9.10(a). This HetJ TFET [285] has an obvious increment on I_{on} (2.7 times) and decrement on τ (from 0.57 to 0.31 ps) and PDP (from 0.81 to 0.70 fJ/μm) compared with its planar ML HomJ SnS counterpart at L_g = 10 nm (see Fig. 9.10(b–d)). Inspiringly, I_{on} of this NHetJ TFET with L_g = 10 nm surpasses the ITRS target for the LP device, although its ML HomJ counterpart fails.

LDDOS, together with the spectral currents of the leakage- and maximum-current states of the BL and ML SnS *n*-type HomJ TFETs and BL-ML SnS NHetJ TFET are compared in Fig. 9.11. On the one hand, in the leakage-current state, both the BL-ML SnS NHetJ TFET and ML SnS HomJ TFETs have a higher tunneling barrier height for electrons than the BL SnS HomJ TFETs, resulting in a lower spectral current peak. Hence the former two TFETs have a lower leakage current. On the other hand, in the maximum-current state, both the BL-ML SnS NHetJ TFET and BL SnS HomJ TFETs have a lower tunneling barrier height for electrons than the ML SnS HomJ TFETs, resulting in a higher spectral current peak. Hence the former two TFETs have a higher maximum current. Apparently, the BL-ML SnS NHetJ TFET combines the advantages of the two HomJ TFETs and owns a higher tunneling barrier height in the off state and a lower tunneling barrier height in the on-state, leading to an improved device performance relative to the latter two.

9.3.4. 2D BP/InSe vdW HetJ thinTFETs

The vdW ML BP/InSe HetJ has a type-II band (staggered) edge alignment, where the valance and conduction bands mainly contribute by the BP and InSe components, respectively. Such a band alignment will allow a large tunneling current because the tunneling occurs from the valence band of ML BP to the conduction band of ML InSe, and thus the barrier height is smaller than those of pristine ML BP and ML InSe [9].

The ML BP/InSe vdW (vertical) HetJ thinTFETs are built, where the optimal device has a 1 nm HetJ at the channel's left and right sites (1L and 1R for short), as shown in Fig. 9.12(a). The BP/InSe HetJ TFETs [286] with the 1L and 1R configurations show *n*- and *p*-type character, respectively, and high I_{on} of 240 and 408 μA/μm are obtained for the HP application at V_{dd} = 0.3 V at I_{off} = 0.1 μA/μm. The high I_{on} arises from the narrow transport barrier by the vdW BP/InSe HetJ, and the *n*- and *p*-type character come from the descending conduction band edge and lifting valence band edge with respect to the ML InSe and BP for 1L and 1R configurations, respectively. Remarkably, I_{on} of the *p*-type ML BP/InSe vdW HetJ thinTFET with 1R configuration is 408 μA/μm at I_{off} = 0.1 μA/μm, greatly surpass those of the pristine GeSe and BP HomJ TFETs and even the strained ML BP TFETs, as shown in Fig. 9.12(b). Hence, the HetJ thinTFET with type-II band alignment indeed has an advantage over the HomJ TFET counterpart.

The band alignment in the NHetJ TFET is type-I band alignment (straddling) based on the fact that the bandgap center of a multilayer 2D material is close to that of an ML 2D material [112]. Taken together, both type-I and type-II band alignment can boost the on-state current for the 2D TFETs. In III–V heterostructures, the tunneling current can be increased by taking both type-II and type-III (broken) band alignment [9,287]. Hence, it is interesting to examine theoretically whether type-III band alignment can improve the device performance of the 2D TFETs.

9.3.5. Indicator for the screening of ML channels for planar HomJ TFETs

The bandgap affects the transport gap, and the average effective mass ($\sqrt{m_e \cdot m_h}$) along the transport direction represents the effective carrier velocity, which leads to an inverse exponential relation of the transmission coefficient (*i.e.*, I_{on}) to the $\sqrt{E_g}$ and $\sqrt[4]{m_e \cdot m_h}.I_{on}$ versus $\sqrt{E_g}$ and $\sqrt[4]{m_e \cdot m_h}$ of several optimal 2D planar HomJ TFETs for the HP application

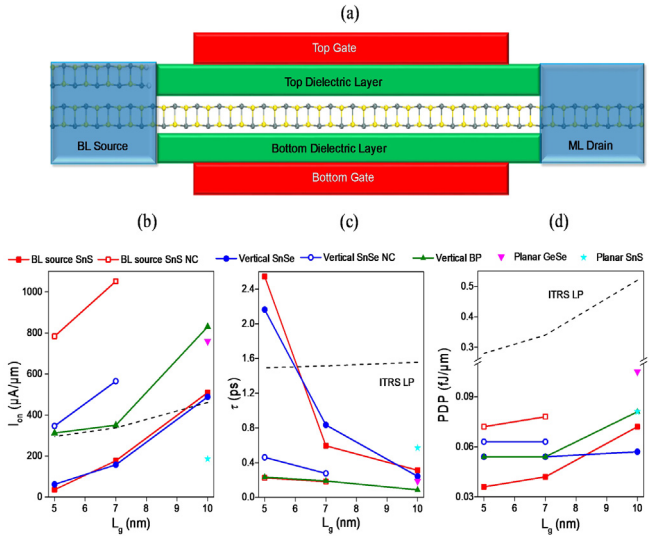


Fig. 9.10. (a) Device model of the SnS NHetJ TFET. (b) I_{on}, (c) τ, and (d) PDP as a function of L_g of the optimal sub-10 nm SnS n-HetJ TFET (solid red squares) and n-NHetJ NCTFET (empty red square) and comparison with the ITRS requirements for the LP devices and several 2D TFETs.
Source: Reproduced from Ref. [285].

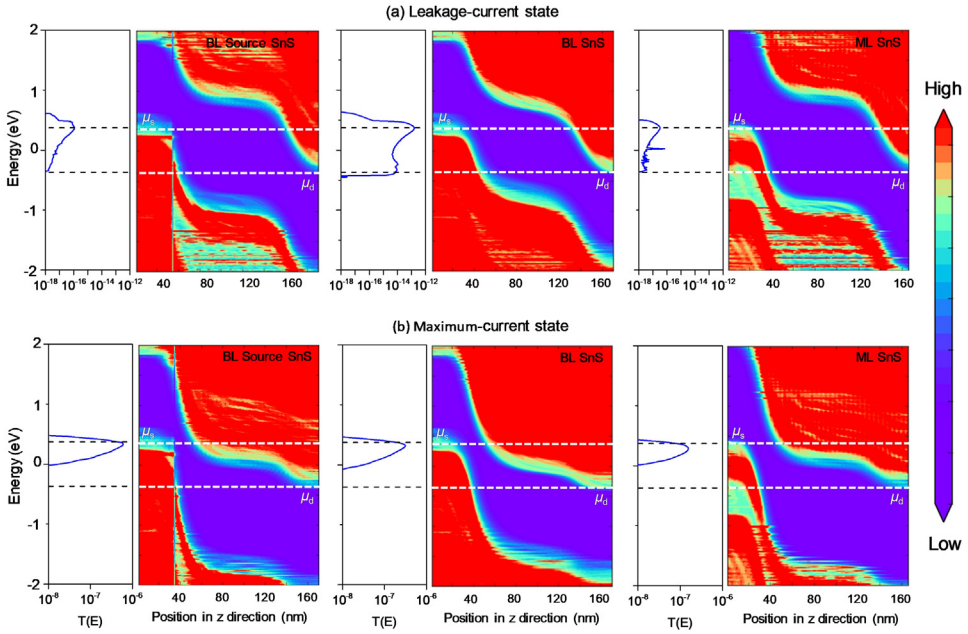


Fig. 9.11. Comparison of LDDOS and spectral currents between BL and ML SnS n-type HomJ TFETs and BL-ML SnS NHetJ TFET with $L_g = 10$ nm at $V_{dd} = 0.74$ V at the (a) leakage-current state and (b) maximum-current state.
Source: Reproduced from Ref. [285].

[283] are given in Fig. 9.13(a) and (b), respectively. The fitting exponential delay relations are $I_{on} = 1.05 \times 10^6 \cdot e^{-6.72\times\sqrt{E_g}}$ and $I_{on} = 5.10 \times 10^5 \cdot e^{-9.77\times\sqrt[4]{m_h \cdot m_e}}$, respectively, which suggests a smaller E_g and $\sqrt{m_e \cdot m_h}$ for a higher I_{on}.

Experimentally, the strained bulk Ge TFET with a small bandgap ($E_g = 0.4$ eV) has a larger I_{on} than the bulk Si TFET ($E_g = 1.17$ eV), confirming that a small gap favors a high I_{on} [288] in a TFET. I_{on} of the ML SnSe, GeSe, and BP TFETs are large enough to surpass the ITRS HP target due to their smaller bandgap. Li et al. suggest a scope of 0.77 – 1.19 eV for E_g and 0.11 – 0.15 m_0 for $\sqrt{m_e \cdot m_h}$ based on the above three excellent channels, with a deviation tolerance of ±0.1 eV and $\pm 0.01 m_0$, to screen a competitive 2D channel for the planar HomJ TFETs [283]. However, in principle, a higher I_{on}

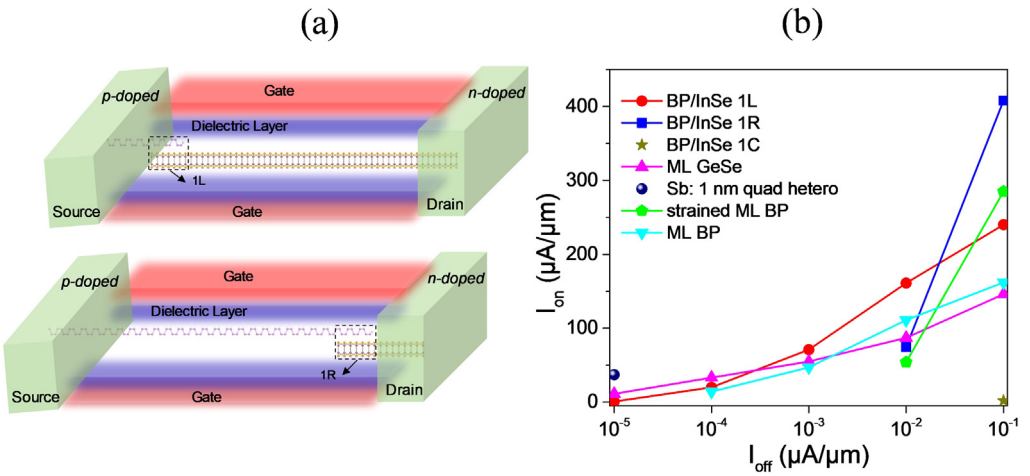


Fig. 9.12. DG ML BP/InSe vdW HetJ thinTFETs: (a) Schematic device model with 1 nm overlap region at the left (upper panel) and right (lower panel) sites. (b) I_{on} *vs.* I_{off} compared with several 2D planar HomJ TFETs at $V_{dd} = 0.3$ V.
Source: Reproduced from Ref. [286].

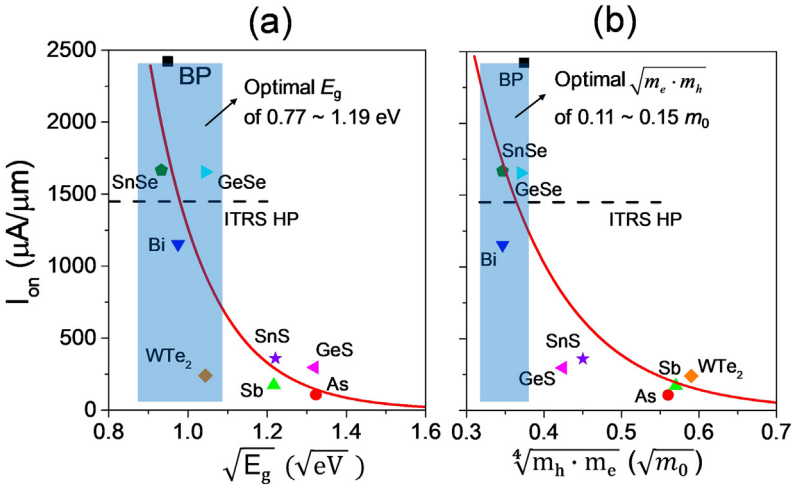


Fig. 9.13. (a) I_{on} (HP) *vs.* $\sqrt{E_g}$ and (b) I_{on} (HP) *vs.* $\sqrt[4]{m_e \cdot m_h}$ for the optimal 2D planar HomJ TFETs at $L_g = 10$ nm. The red lines denote the fitting exponential curves.
Source: Reproduced from Ref. [283].

can be expected if a 2D material has a smaller E_g (< 0.77 eV) as long as the leakage current can meet the ITRS criterion. It is interesting to check such an inverse dependence of I_{on} on E_g and $\sqrt{m_e \cdot m_h}$ can be expanded to the HetJ TFETs.

10. Sub-10 nm negative capacitance FET (NCFET)

10.1. Negative capacitance working mechanism

As Moore's law goes on, the further downscaling of MOSFET has been hindered because the threshold voltage cannot be lowered due to the Boltzmann tyranny [215,289]. Researchers have to explore novel sharp switching devices with different work mechanisms. Among the candidates, negative capacitance (NC) FET has been considered a promising option [290,291].

According to the Landau theory, during two different polarization transitions, an energy barrier appears, and this makes the ferroelectric material show the negative capacitance phenomenon in an unstable state, as shown in Fig. 10.1(a). When we apply a voltage on the ferroelectric material, the energy structure gets tilted, and the polarization will transfer to the nearest stable state with the minimum energy; during this process, it may pass through the negative capacitance state (strictly, negative differential capacitance) around $P = 0$ (the red dashed curve in Fig. 10.1(b)) [292,293]. However, with

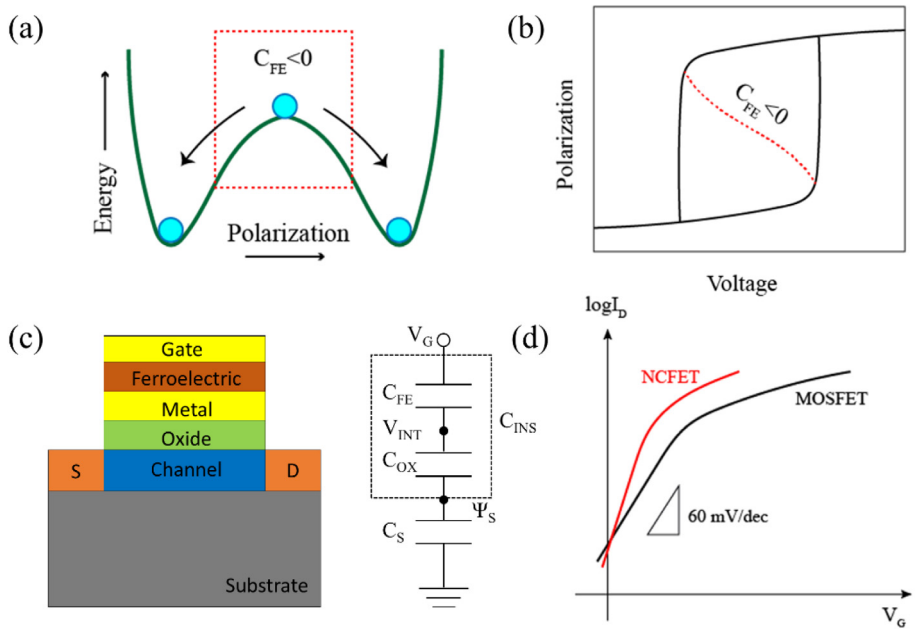


Fig. 10.1. (a) Unstable polarization negative capacitance state in the energy landscape of a ferroelectric material. (b) Typical polarization-voltage curves of a ferroelectric material. The capacitor exhibits a negative when it is in an unstable polarization state. (c) Sectional schematic of a typical NCFET device structure, which has a metal–ferroelectric–metal–oxide–semiconductor structure. The equivalent capacitor circuit is also shown on the right, where C_{FE}, C_{ox}, and C_s represent the capacitance of the ferroelectric, oxide, and semiconductor.V_{int} and Ψ_S are the internal voltage and surface potential of the channel. (d) Typical transfer curves of an NCFET and conventional MOSFET are plotted in the same coordinate.

a series dielectric capacitor, this unstable negative capacitance state can be stabilized possibly. Following this idea, Datta et al. proposed that by replacing the standard gate oxide with a ferroelectric insulator in a FET configuration, it is possible to step up the gate voltage and obtain a sub-60 mV/dec feature [294]. Such a FET is referred to as negative capacitance FET (NCFET). A typical NCFET structure is shown in Fig. 10.1(c), and its equivalent capacitor model is also shown as it is more intuitive to understand its working mechanism. The critical factor characterizing a FET's switching speed is the subthreshold slope *SS*, which is defined as follows,

$$SS = \frac{\partial V_G}{\partial \log_{10} I} = \frac{\partial V_G}{\partial \Psi_s}\frac{\partial \Psi_s}{\partial \log_{10} I}$$

where V_G, Ψ_s and I represent the gate voltage, surface potential, and drain current, respectively.

$\partial\Psi_s/\partial \log_{10} I$ is always equal or larger than 60 mV/dec at room temperature due to the "Boltzmann tyranny". V_G and Ψ_s have the following relation deducted from the capacitive voltage dividing model,

$$\frac{\partial V_G}{\partial \Psi_s} = 1 + \frac{C_S}{C_{INS}}$$

Because C_{INS} is equal to $C_{FE}C_{OX}/(C_{FE}+C_{OX}) < 0$, $\partial V_G/\partial \Psi_s$ is less than 1, which means that *SS* can be smaller than the thermal limit of 60 mV/dec.

10.2. Experimental long 2D NCFETs

Transistors based on the working mechanism of negative differential capacitance have been implemented since 2008. Salvatore et al. experimentally demonstrated negative capacitance transistors for the first time [295]. 40 nm P(VDF-TrFE) was integrated into the gate stack of traditional bulk silicon transistors, and an *SS* of 13 mV/dec was obtained, as shown in Fig. 10.2(a) and (b). In addition to the bulk silicon, the integration of ferroelectric materials can also be realized on Si-fin (Fig. 10.2(c)). Li et al. used Zr-doped hafnium oxide as a ferroelectric layer and Si-fin as the channel [296]. The channel's surface potential was amplified by 1.6 times, *SS* was reduced to 55 mV/dec, and the on-state current had also been increased by 25%. This work firstly shows the implementation of a negative differential mechanism to advanced Si-fin. It is compatible with the existing silicon technology and also provides the possibility of continuing Moore's law. Besides traditional silicon materials, negative capacitance mechanism has also been applied to 2D materials. A.D. Franklin et al. used $HfZrO_2$ as a ferroelectric layer and MoS_2 as channel material [297]. In this work, *SS* can be kept at 8.03 mV/dec for four orders of magnitude (Fig. 10.2(e) and (f)). As mentioned above, the NCFET technology has become mature gradually in the experiment due to its compatibility with mainstream technology and feasibility.

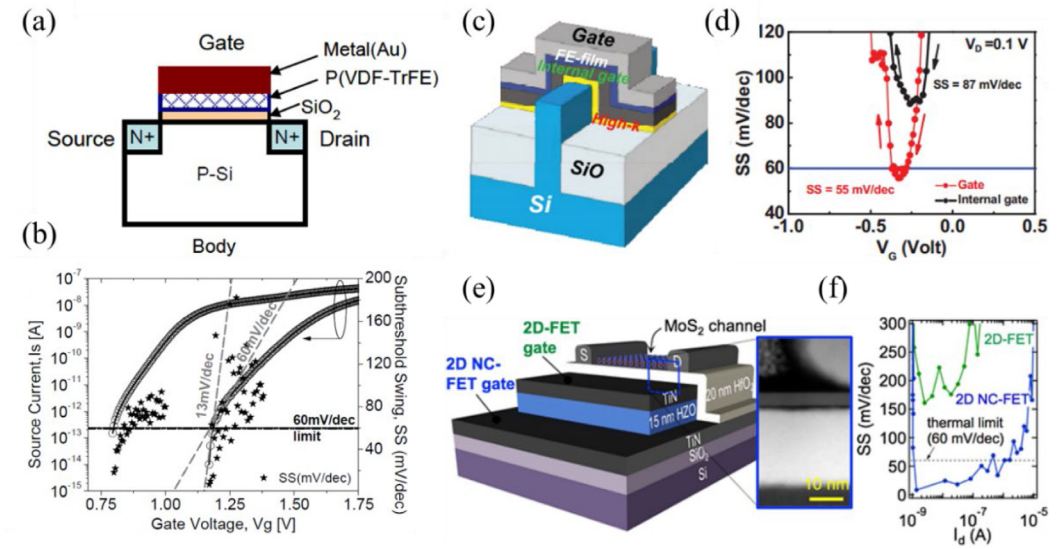


Fig. 10.2. (a) Device structure of the ferroelectric transistor. (b) Subthreshold swing analysis. The star points show the *SS* for source current data [295]. (c) The device structure of NC-FinFET. (d) Comparison between *SS* of *p*-type NC-FinFET and internal FinFET [296]. (e) 2D NC-FET device configuration and (f) extracted *SS* from the 2D-FET and 2D NC-FET [297].
Source: (a) and (b) reproduced from Ref. [295]. (c) and (d) reproduced from Ref. [296]. (e) and (f) reproduced from Ref. [297].

Though several groups have fabricated NCFETs or observed the negative capacitance effect in the experiment, an experimental 'S' shaped P–E curve had not been demonstrated until recently [290,298,299]. In 2018, Michael Hoffmann et al., for the first time, unveiled the intrinsic double-well energy landscape in $Hf_{0.5}Zr_{0.5}O_2$ [300]. They integrated the ferroelectric into the capacitor with a dielectric Ta_2O_5 layer and used pulsed charge–voltage measurements to mitigate the screening of the polarization charge, as shown in Fig. 10.3(a), and their results showed that the negative capacitance originated from the energy barrier in the double-well landscape (Fig. 10.3(c) and (d)), which is buttressed by countless simulations. Furthermore, they also demonstrated that the negative capacitance of the ferroelectric could have a hysteresis-free operation even at an applied pulse of 100 ns, and this is important in high-speed digital applications.

10.3. Sub-10 nm 2D NCFET simulations

Sub-60 mV/dec was presented in the long-channel NCFETs, but the NCFETs of the short channel below 10 nm have not been obtained at the experimental level. Nevertheless, some simulations without suffering from technical problems go ahead. Harshit Agarwal et al. designed 5 nm NC-FinFET by solving the BSIM-CMG compact model and Landau–Khalatnikov (LK) equation, and the designed transistor can both meet the low-power and high-performance targets at 0.23–0.5 V working voltage [301]. Besides, they showed that changing the parasitic capacitance and ferroelectric coercive field can optimize the device performance and achieve the best design. Apart from the conventional Si channel material, sub-10 nm NCFETs based on 2D material such as ML BP and tellurene were also explored. In one work, quantum transport properties of 2D NCFETs with ML BP were theoretically calculated [302]. They showed that the atomic thin BP channel could enhance the amplify effect of the ferroelectric layer, and *SS* can decrease to 27 mV/dec in Fig. 10.4(b). The characteristics of scaling behavior and sub-10 nm BP NCFETs were also investigated. *SS* decreases quickly when the channel length is reduced (Fig. 10.4(a)). Compared to DG FETs, NCFETs can work at a lower work voltage of 0.3 V and reduce power consumption.

In another study, the performance limit of the DG ML tellurene MOSFETs with a sub-5 nm gate length (Fig. 10.4(c)) is investigated by *ab initio* quantum transport simulations, and combined with LK equation, the transfer characteristics of sub-5 nm tellurene NCFETs are also calculated [244]. With the 100 nm HZO imposed into the gate stack, the optimized *p*-type DG NCFETs base on ML tellurene meet both the LP and HP ITRS requirements while the gate length is reduced to 4 nm, as shown in Fig. 10.4(f). These theoretical calculations show the promising prospect of integrating the NC effect into MOSFET at the sub-10 nm gate-length node.

10.4. Experiments and simulations of NCTFETs

To achieve a double-steep slope transistor, integrating the ferroelectric into a tunnel transistor would be a practical and feasible option. The tunnel FET is based on the band-to-band tunneling (BTBT) transport to break the fundamental

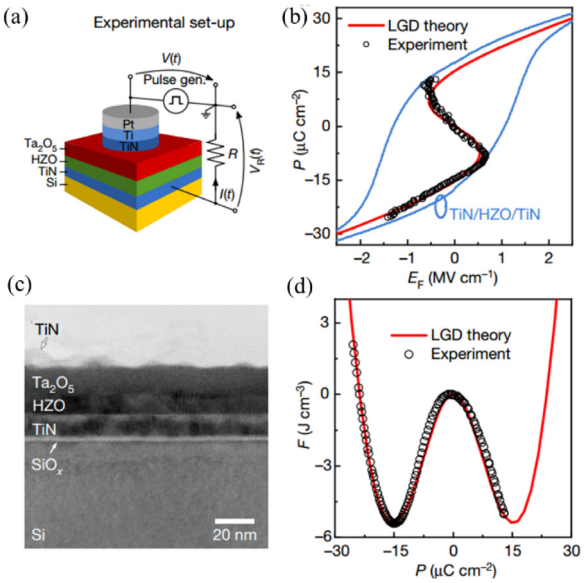
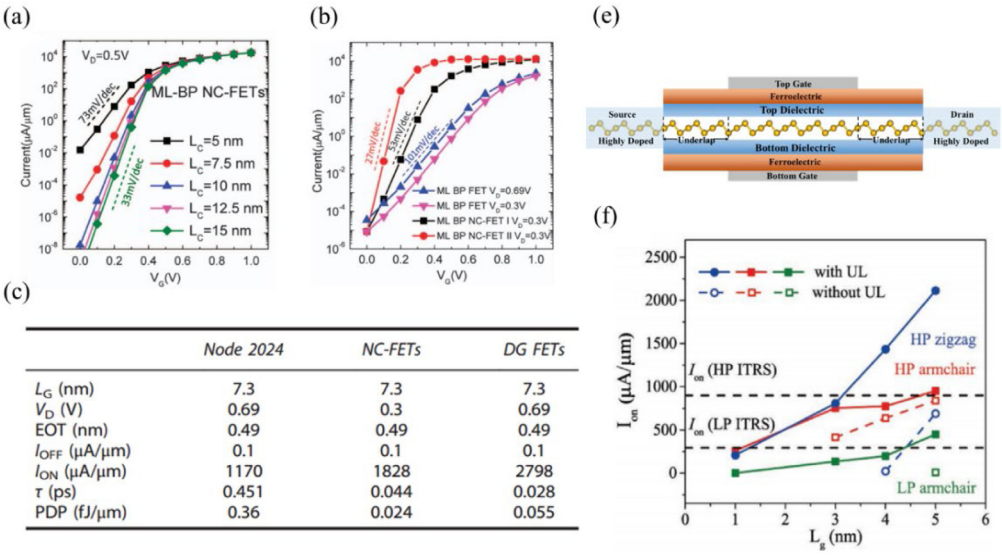


Fig. 10.3. (a) Schematic experimental set-up of measuring the pulsed charge–voltage characteristic [300]. Transmission electron microscopy (TEM) picture of the $TiN/Ta_2O_5/Hf_{0.5}Zr_{0.5}O_2/TiN$ structure-based capacitor. (c) Polarization–electric field relationship of the $Hf_{0.5}Zr_{0.5}O_2$ layer with a fit curve based on LGD theory. (d) Result of integrating the P–EF characteristics in (c).
Source: Reproduced from Ref. [300].



(c)

	Node 2024	NC-FETs	DG FETs
L_G (nm)	7.3	7.3	7.3
V_D (V)	0.69	0.3	0.69
EOT (nm)	0.49	0.49	0.49
I_{OFF} (μA/μm)	0.1	0.1	0.1
I_{ON} (μA/μm)	1170	1828	2798
τ (ps)	0.451	0.044	0.028
PDP (fJ/μm)	0.36	0.024	0.055

Fig. 10.4. (a) Transfer curves for ML BP NCFETs with 3 nm HfO_2 layer, 400 nm ferroelectric layer, and channels of different length at supply voltage of 0.5 V. (b) Transfer curves for ML BP NCFETs and ML BP FETs with a HfO_2 layer of 3 nm and a channel length of 7.3 nm. NC-FETs I and II have a ferroelectric layer of 400 and 600 nm, respectively. (c) DG FETs based on ML BP and ML BP NCFETs with a ferroelectric layer of 400 nm against the HP requirements of ITRS [302]. (e) Schematic of the DG NCFET based on ML tellurene. (f) On-state current versus the gate length for the sub-5 nm *p*-type DG MOSFETs based on ML tellurene without UL (open symbol) and with an optimized UL (solid symbol) [244].
Source: (a)–(c) are reproduced from Ref. [302]. (e)–(f) are reproduced from Ref. [244].

thermal limitation. The general formula for the subthreshold swing of a transistor is

$$SS = \frac{\partial V_G}{\partial \log_{10} I} = \frac{\partial V_G}{\partial \Psi_s}\frac{\partial \Psi_s}{\partial \log_{10} I} = (1 + \frac{C_S}{C_{INS}})\frac{\partial \Psi_s}{\partial \log_{10} I} = m \cdot n \tag{10.1}$$

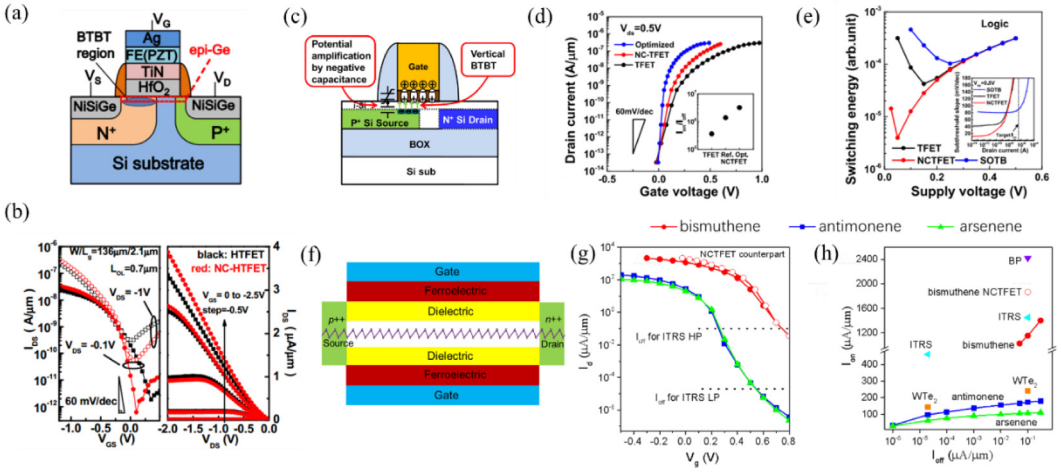


Fig. 10.5. (a) Schematic structure of NC-HTFET [303]. (b) Experimental transfer characteristic and output characteristic of NC-HTFET. (c) Schematic of the simulated NCTFET. (d) Transfer curves of an optimized NCTFET as well as the reference NCTFET and TFET. (e) Energy efficiency of optimized NCTFET, TFET, and SOTB for logic operations [304]. (f) Schematic of TFETs based on ML hexagonal V-ene. (g) Transfer curves of the three checked TFETs based on ML hexagonal V-ene and the NCTFET based on ML bismuthene with a gate length of 10 nm. (h) I_{on} *vs.* I_{off} of the NCTFET based on ML bismuthene and the three checked TFETs based on ML V-ene against LP and HP requirements of ITRS and those of the TFETs based on ML BP and ML WTe_2 [305].
Source: (a)–(b) are reproduced from Ref. [303]. (c)–(e) are reproduced from Ref. [304]. (f)–(h) are reproduced from Ref. [305].

where $m = 1 + \frac{C_S}{C_{INS}}$ and $n = \frac{\partial \Psi_S}{\partial \log_{10} I}$. The NC mechanism leads to the body factor m less than 1, and the tunneling operation is beneficial for n-term less than 60 mV/dec. With the coupling of a ferroelectric with a tunnel transistor, *SS* can be doubly reduced. This concept was first proposed and performed by Lee et al. in the experiment [303]. They fabricated an NC hetero-tunnel FET (NC HTFET) with 7.8 nm HfO_2 as the gate dielectric and 30 nm $PbZrTiO_3$ (PZT) as the ferroelectric layer, as shown in Fig. 10.5(a). The transfer curve of NC HTFET showed enhancement in the SS, *i.e.*, the 100–200 mV/dec *SS* of HTFET was reduced to 60 mV/dec with the internal voltage application of the NC effect in Fig. 10.5(b). The on-state current was also improved in the output characteristics of NCHTFET, with 118% peak transconductance improvement compared to HTFET.

Aside from the experimental studies, simulations of NCTFETs also take a step. Ali et al. studied the capacitance matching in NCTFETs and found that in the non-hysteretic NCTFET case, the on-state current was improved by 500 times, transconductance was also enhanced by three orders of magnitude, and extension of the low *SS* was also obtained [306], while the boosting of performance in the hysteretic NCTFET is just moderate and has no *SS* improvement. In another research, the NC effect is integrated into a vertical TFET (VTFET), as shown in Fig. 10.5(c) [304]. VTFET benefits from the more efficiently-tuned potential at the tunnel junction than lateral TFET and has a larger on-state current. They combined the TCAD simulation and LK equation to include the NC amplification. Different parameters were adjusted like the source doping, overlap between the gate and the source, the gate insulator's thickness, and other ferroelectric layer properties, and an optimized NCTFET was obtained. The optimized NCTFET shows the highest on/off ratio among the reverence NCTFET and TFET. Besides, the switching energy of different devices was also analyzed, and for both logic and memory applications, NCTFET has a lower energy minimum voltage and can enhance more than 10 times the energy efficiency compared with TFET and MOSFET at supply voltage less than 0.2 V in Fig. 10.5(e).

In addition to traditional materials, *ab initio* quantum transport simulations method was adopted to study the DG ML bismuthine MOSFETs' device performance with a gate length of 10 nm and combined with the LK equation, the transfer characteristics of ML bismuthine NCFETs were also obtained [305]. With the 100 nm HZO imposed into the gate stack, the *SS* of the bismuthine NCFETs is improved from an average value of 184 to 145 mV/dec. The on-state current was also increased to 1868 μA/μm and fulfilled the HP requirements (1450 μA/μm) in the ITRS, as shown in Fig. 10.5(g) and (h), and the on-state performance was up to half of the ML BP TFET counterpart [216]. These theoretical calculations show the prospect of integrating the NC effect into TFET for the ultra-low-power IoT technology.

11. Sub-10 nm carbon nanotubes (CNT) FETs

11.1. Fundamental properties of CNTs

Carbon nanotubes (CNTs) are discovered by Iijima et al. in 1991 [307] and formed by rolling up ML graphene sheets into a hollow cylinder. The electrical properties of CNTs depend on how the graphene sheets roll up by a chiral vector during the growth process, as shown in Fig. 11.1, and these (n, m) CNTs (n, m are positive integers) can either exhibit

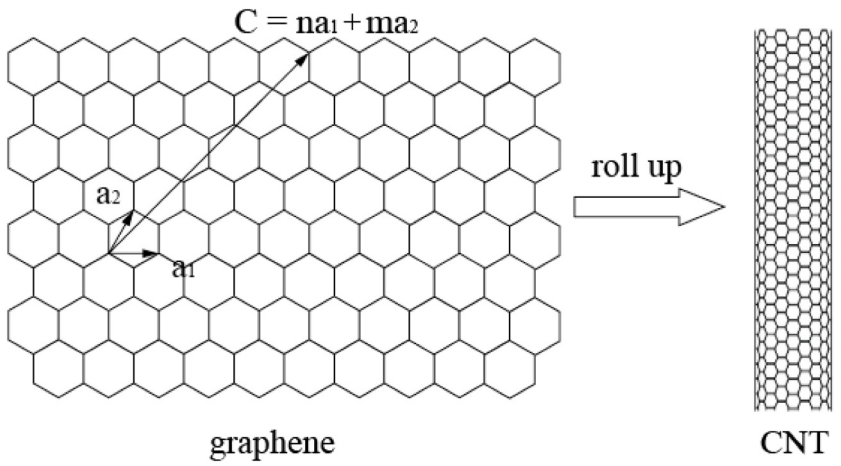


Fig. 11.1. Diagram showing the graphene sheet curled into a CNT by the direction of a chiral vector. The chiral vector $C = na_1 + ma_2$, where a_1 and a_2 are unit vectors of the graphene lattice.

semiconducting or metallic conducting behavior according to their chirality. If $(n - m)$ is an integer multiple of 3 or 0, the CNT is metallic; otherwise, it is semiconducting. The chirality also determines the diameter (d_{CNT}) of CNTs and $d_{\mathrm{CNT}} = a\sqrt{n^2 + nm + m^2}/\pi$, where a is the Bravais lattice constant. Diameter is an important physical parameter, and it is inversely proportioned to the bandgap of CNTs.

Different from zero-bandgap graphene, semiconducting CNTs of appropriate diameter have a bandgap suitable for electronic applications. CNT FETs are promising for conventional MOSFETs. With 1–3 nm diameters, carbon nanotube has a quasi-one-dimensional (1D) body, and this ultra-thin body help achieve high gate efficiency and thus makes it short-channel-effects-immune. With the ultra-high mean free path of hundred nanometers and mobility of 10^5 cm ^{2}/(V·s) at room temperature, it can realize 1D quasi-ballistic transport and high drive current. The symmetry of conduction and valence band structure leads to a perfect symmetry NMOS and PMOS performance at the same device sizes, which is impossible for silicon-based transistors. Above all, as a channel material, CNTs have vital natural factors for better downscaling potential and LP applications [308–312].

11.2. Experimental long CNT FETs

The first CNT FET in a typical three-terminal configuration is realized by Dekker et al. at Deft University and Avouris et al. at IBM Research Division in 1998 [313,314], where semiconducting CNTs are placed between Pt or Au electrodes and the back gate is doped Si substrate. Although the transistors' performance is bad, *i.e.*, the output conductance is only 0.65% of the ballistic quantum conductance due to the absence of ohmic contact and advanced device structure, the on/off ratio of these FETs can be modulated with the back gate by more than 5 orders of magnitude as shown in Fig. 11.2(b), which represents an important step towards carbon-based electronics.

Besides success in device fabrication, a theoretical understanding of the underlying operation of CNT FETs has been obtained by researchers at IBM [315]. Different from conventional MOSFETs with the doped source (drain), CNT FETs with non-ideal metal contact operates as SBFETs, where the gate mainly changes the contact resistance through modulating SB thickness at the contact interface rather than channel conductance as shown in Fig. 11.2(c) and (d). The current through the CNT channel reduces exponentially with increasing SBs height and thickness at the metal-tube interface. Therefore, Ohmic contact needs to be achieved for high drive capability.

In 2003, Ali et al. found that Pd can form an ideal p-type Ohmic contact with the CNTs [310]. In Fig. 11.3(b) and (c), the on-state conductance of CNT FETs with Pd contact was up to 10% and 40%–50% of the ballistic limit ($G_0 = 4e^2/h$) for the long-diffusive and short quasi-ballistic channel, respectively. However, n-type high-performance CNT FETs with Ohmic contact were not realized because of the absence of a reliable and controllable doping technique. In 2007, Zhang et al. firstly used Sc as the contact and successfully fabricated ballistic n-type CNT FETs in the back gate device structure [316]. Metal Sc can form perfect contact with the CNT due to its good wetting property, as shown in Fig. 11.3(d), which leads to an Ohmic contact and high conductance ($G = 0.49G_0$) at 250 K, as shown in Fig. 11.3(e). A gate stack is as essential as a contact in transistors, and an appropriate gate stack can lead to high gate efficiency and good device stability. Besides the electrical contacts, researchers explored a series of high-κ gate dielectric material and gate structure to optimize the CNT FETs' performance [317–319].

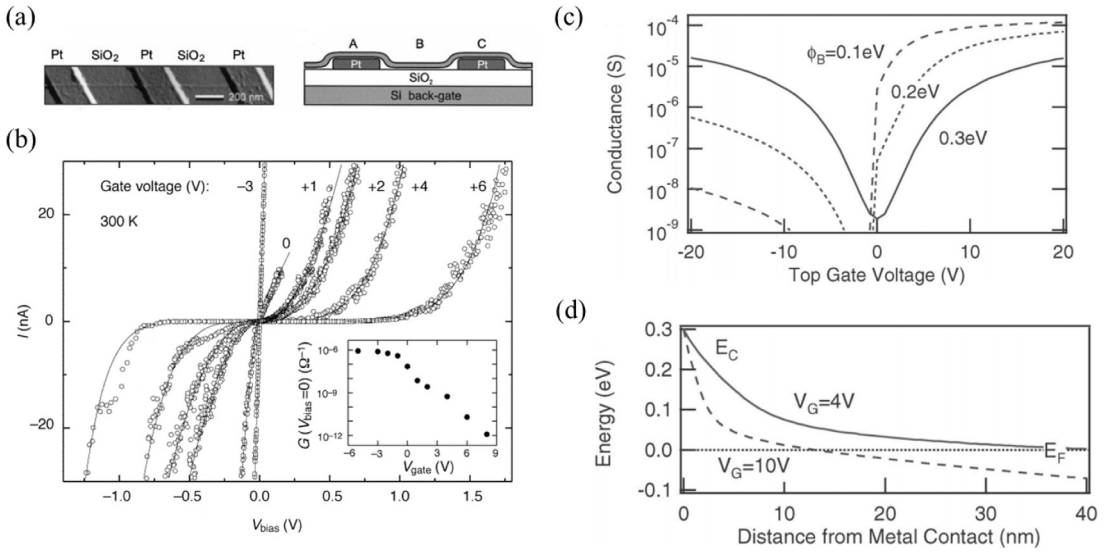


Fig. 11.2. (a) Atomic force microscope (AFM) image of a single CNT on top of three Pt electrodes and the side view of the device. (b) I–V_{bias} curves under different gate voltage [314]. (c) Device conductance versus the gate voltage at room temperature for different SBs. (d) CNT conduction band energy distribution near the contact under gate voltage of 4 and 10 V [315].
Source: (a)–(b) are reproduced from Ref. [314]. (c)–(d) are reproduced from Ref. [315].

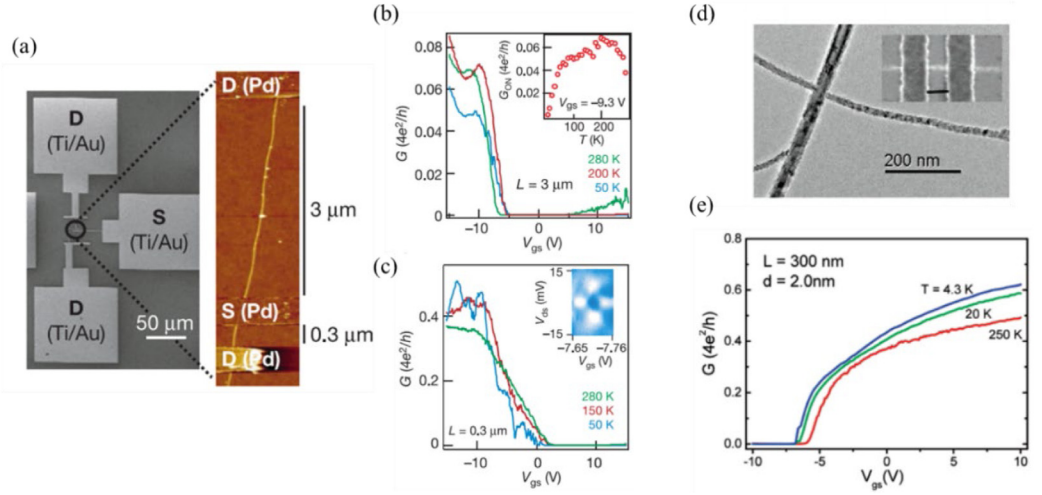


Fig. 11.3. (a) Back-gated CNT FETs (L = 300 nm and L = 3 mm) with Pd contact are fabricated on the same CNT. (b) Conductance as a function of the gate voltage for a 3 μm-long CNT FET at different temperatures T. (c) Conductance versus gate voltage for a CNT FET with a gate length of 300 nm at various T [310]. (d) TEM results show that the CNTs are uniformly coated by Sc. (e) Conductance as a function of the gate voltage for a CNT with a length of 300 nm and a diameter of 2.0 nm at a low bias voltage of 0.1 V [316].
Source: (a)–(c) are reproduced from Ref. [310]. (d)–(e) are reproduced from Ref. [316].

11.3. Experimental sub-10 nm CNT FETs

In 2012, the first sub-10 nm carbon nanotube transistor was explored in the experiment by Aaron et al. [320]. The device had a back-gated geometry with local bottom gates, and it was capped by a 3 nm HfO_2 gate oxide in Fig. 11.4(a). Even if the device structure was primitive, the first sub-10 nm CNT transistor was shown to perform better than the best silicon FETs by more than four times in terms of on-state current density at V_{DD} of 0.5 V, and *SS* of 94 mV/dec was obtained as shown in Fig. 11.4(b).

In 2017, the research of the sub-10 nm CNT FETs had taken another step forward. Advanced top-gated CNT FETs with gate length scaled below 10 nm were successfully fabricated by Qiu et al. [51]. For the 10 nm gate-length *p*- and *n*-type CNT FETs with Pd (Sc) as sources (drains) and 3.5 nm HfO_2 as gate dielectric, an ideal subthreshold swing of 70 mV/dec was obtained. The on-state current is as high as 0.76 mA/μm at the bias voltage of 0.4 V (Fig. 11.4(c)) for the *p*-type CNT

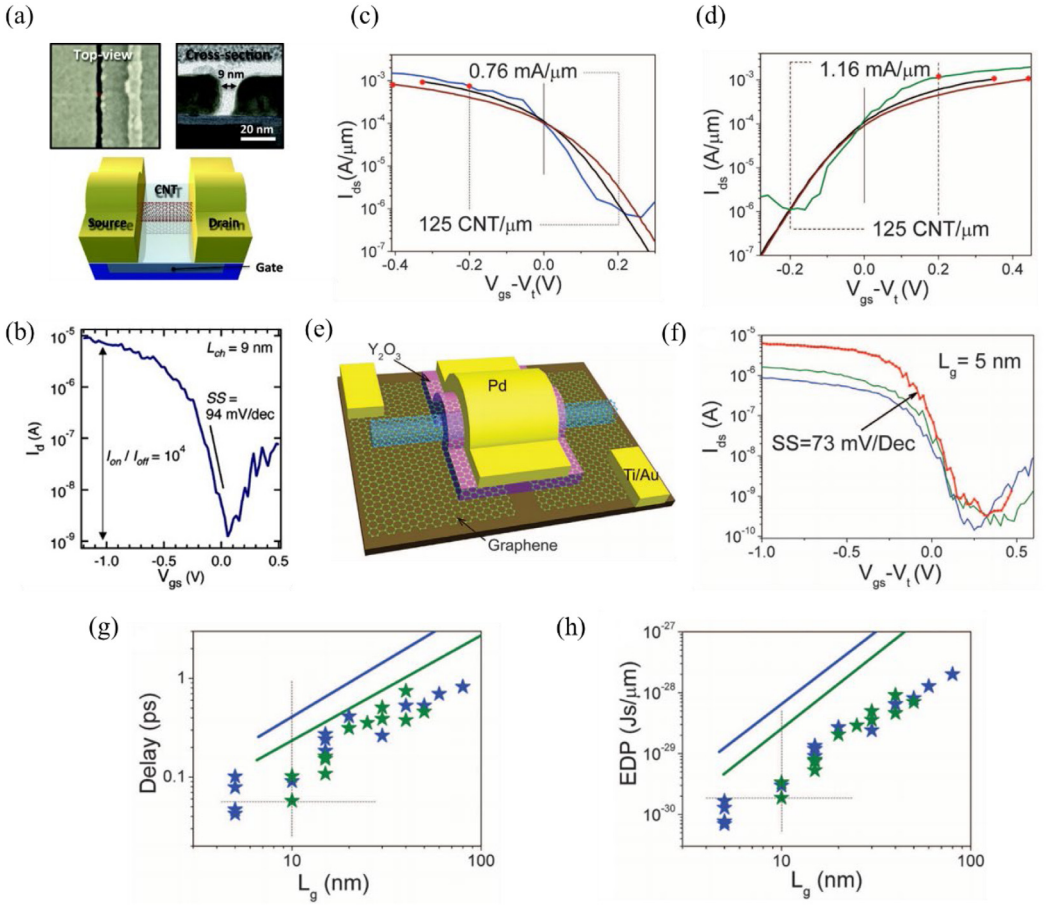


Fig. 11.4. (a) Sub-10 nm CNT FET device structure with top-view and side-view electron microscope images. (b) A typical transfer curve of a sub-10 nm CNT FET under $V_{ds} = -0.4$ V [320]. (c–d) 10 nm CMOS FETs based on CNT against commercial Si CMOS transistors of Intel's 22 nm nodes (solid maroon curve) and 14 nm (solid black curve). (e) Schematic of a CNT FET with graphene contacts. (f) Transfer curves of three typical graphene-contact CNT FETs with $L_g = 5$ nm show *SS* of 73 mV/decade at $V_{ds} = -0.1$ V. Scaling behavior of the gate delay (g) and EDP (h) of the Si CMOS FETs and CNT CMOS FETs. The *n*-type and *p*-type MOSFETs based on Si are in solid olive line and blue line, respectively. The *n*-type and *p*-type FETs based on the CNT are in olive and blue stars in all panels, respectively [51].
Source: (a)–(b) are reproduced from Ref. [320]. (c)–(h) are reproduced from Ref. [51].

FET and 1.16 mA/μm (Fig. 11.4(d)) for the *n*-type CNT FET, exhibiting a higher I_{on} at a much smaller V_{DD} compared to the highest-performing Si counterparts.

With graphene as the electrode, the CNT FET with 5 nm gate length has also been fabricated by Peng et al., as shown in Fig. 11.4(e). An ideal *SS* of 73 mV/dec was observed, and it was much better than that (208 mV/dec) of the Si FETs with the same gate length of 5 nm. The benchmark of the CNT FETs against the Si counterparts in the gate delay and energy-delay product are shown in Fig. 11.4(g) and (h). Both the *p*- and *n*-type CNT FETs outperform the Si FETs with gate lengths ranging from 5 to 100 nm under a smaller V_{DD} of 0.4 V in terms of both the switching speed and energy-delay product. For example, the 10 nm CNT CMOS FETs have EDPs as low as 1.88×10^{-30} Js/μm, which is about one order of magnitude lower than the predicted limit of a Si *n*-type FET at the end of ITRS.

11.4. Simulations of sub-10 nm CNT FETs

In addition to the experimental research, there were also several theory studies of the ultra-scaled CNT FETs. Guo et al. used a tight-binding atomistic scale simulation to study the scaling behavior of the CNT SBFETs [321]. They found that ambipolar transport was evident for the devices with metal source and drain when the gate dielectric is very thin. As the gate length was scaled below 10 nm, source–drain tunneling dominated and deteriorated the off-state current. If the 5 nm channel length was adopted, the on/off current ratio of CNT FET could decrease to less than ten due to the severe tunneling leakage current, as shown in Fig. 11.5(b). This decrease mostly attributes to the CNTs' typically smaller bandgaps and lighter effective mass, and using CNTs with smaller diameters can be a solution.

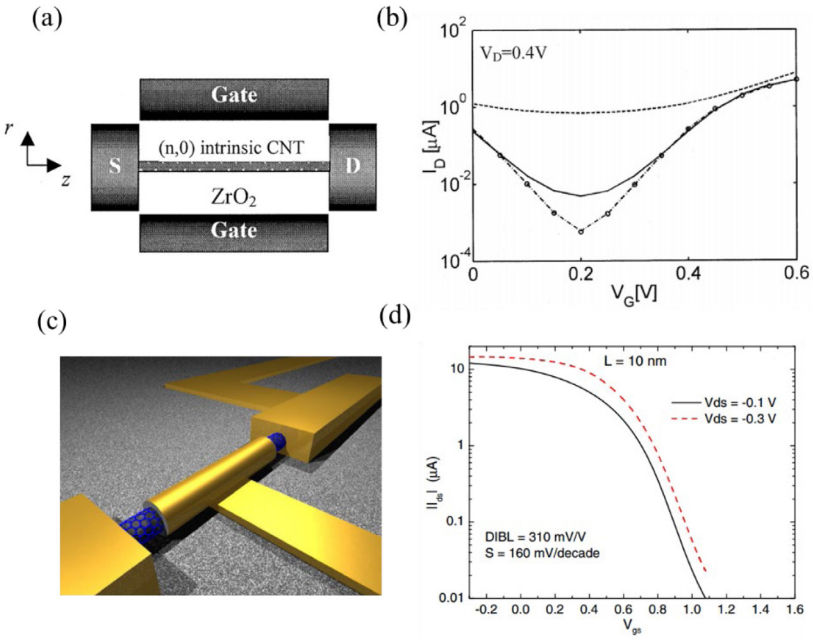


Fig. 11.5. (a) CNT FET with a coaxial gate. The gate length is 15 nm. (b) Transfer characteristics of CNTFETs with different channel lengths. The circles are for channel length $L = 30$ nm and gate oxide ZrO_2 thickness $t = 2$ nm, the dash–dot line for $L = 15$ nm and $t = 2$ nm, the solid line for $L = 10$ nm and $t = 2$ nm, and the dashed line for $L = 5$ nm and $t = 1$ nm. (c) Schematic diagram of the CNT FET. (d) Transfer curves for the CNT FET with a channel length of 10 nm.
Source: (a)–(b) are reproduced from Ref. [321]. (c)–(d) are reproduced from Ref. [322].

In addition to the SBFETs, the CNT FETs with Ohmic contact in a GAA configuration (Fig. 11.5(c)) were studied [322]. It is found that for the short channel CNT based FETs, the tunneling phenomenon and drain-induced barrier lowering effect affect the intrinsic characteristics of the CNTs severely, and a poor *SS* of 160 mV/dec was obtained through the semi-empirical self-consistent NFGF simulation for the 10 nm gate-length device, as shown in Fig. 11.5(d). The GAA CNT MOSFETs with a gate length of 2 nm were studied using a π-bond model and a self-consistent NEGF scheme [323]. Although the gate length is 2 nm, the UL on each side is relatively large. Due to the long UL of 24 nm, the devices behave nicely with a nearly ideal *SS* of 63 mV/dec and a maximum on/off ratio of 2.2×10^6 under 0.4 V voltage swing.

Recently, Xu et al. examine the sub-5 nm gate-length GAA MOSFETs based on the (8, 0) CNT channel extensively by using the accurate *ab initio* quantum transport simulation [324]. The experimental and simulated transfer curves of the 5 nm gate-length SG CNT FET coincide well, as shown in Fig. 11.6(b). Because the simulation is based on the ideal condition (perfect geometry, ballistic transport, and Ohmic contact), such a good agreement validates the high reliability of the state-of-art *ab initio* quantum transport simulation and also shows that the experimental CNT FET has reached the ideal limit.

According to the *ab initio* quantum transport simulation, the CNT MOSFETs cannot reach the ITRS HP requirement in the sub-3 nm gate-length node without device structure modification, and the corresponding *SS* is larger than 300 mV/dec, as shown in Fig. 11.6(c). However, with the aid of 3 nm UL, the CNT MOSFETs can fulfill the ITRS HP requirement even in the ultra-scaled 2 nm gate-length node with a high on-state current of 1340 μA/μm as shown in Fig. 11.6(d). As the gate length is further downscaled to 1 nm, SCEs dominated, dominant tunneling leakage current deteriorates the devices' off-state performance, and even a large UL of more than 3 nm cannot help.

A comparison of the key figures of merit between the advanced Si FETs and CNT FETs at the sub-10 nm region is provided in Table 11.1. The experimental and simulated results 5 nm-L_g CNT FET coincide well in I_{on}, delay time, and PDP. It is worthy to note that both the experimental and theoretical on-state currents of the CNT MOSFETs are superior to those of most of the advanced experimental Si-based transistors, such as UTB SOI FET [169], Si nanowire FETs [325], and Si FinFET [326]. For example, among these Si-based FETs, the best I_{on} of the 10 nm-L_g Si nanowire FET is 522 μA/μm under a V_{dd} of 1V [325], which is smaller than those (1058–1703 μA/μ(m) of the 5 nm-L_g GAA (8, 0) CNT FET under a V_{dd} of 0.64 V. Compared to the Si counterparts, the CNTs have smaller body thickness (1–2 nm), higher mobility (3000 $cm^2/(V\cdot s)$) and longer mean free path (hundreds of nanometers). As a result, the CNT MOSFETs demonstrate better performance in not only I_{on} but also delays (0.02–0.04 ps for the CNT devices versus 0.22–0.62 ps for the Si devices as shown in Table 11.1) and PDPs (0.02–0.034 fJ/μm for the CNT devices versus 0.055–0.316 fJ/μm for the Si devices) in the 5 nm gate-length node.

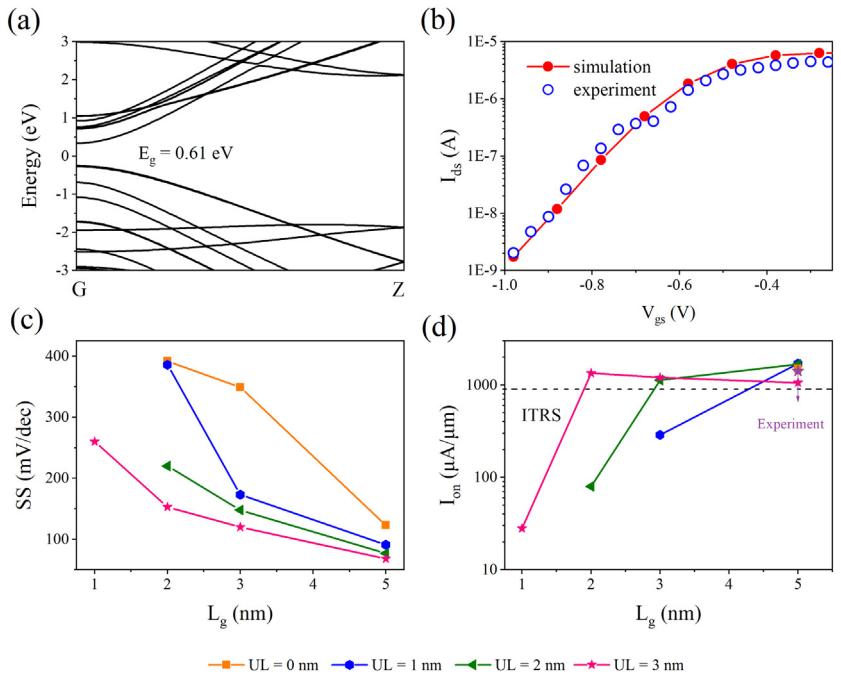


Fig. 11.6. (a) Band structure of the (8, 0) CNT. (b) Experimental and simulated transfer curves of the 5 nm gate-length SG CNT MOSFETs. (c) Subthreshold swing and (d) on-state current as a function of the gate length of the sub-5 nm GAA CNT MOSFETs. The current is normalized by assuming 200 tubes per micrometer [320].

Table 11.1
Benchmark of the ballistic device performances of the sub-5 nm-gate-length GAA CNT MOSFETs against the ITRS requirements for the HP transistors of the next decades (2013 version) and other sub-10 nm-gate-length technologies. The off-current is set to be 0.1 μA/μm (the ITRS HP requirement).

		L_g (nm)	UL (nm)	EOT (nm)	V_{dd} (V)	*SS* (mV/dec)	I_{on} (μA/μm)	I_{off} (μA/μm)	C_g (fF/μm)	τ (ps)	PDP (fJ/μm)
ITRS HP 2028		5.1	–	0.41	0.64	–	900	0.1	0.198	0.14	0.08
Si nanowire [325]		10	–	1.9	1.0	75	522	0.01	0.115	0.22	0.115
Si nanowire [325]		5	–	1.9	1.0	63	115	0.001	0.055	0.48	0.055
Si Fin [326]	Experiment	10	–	1.7	1.2	125	446	1.7	0.126	0.34	0.182
Si Fin [327]		5	–	1.2	1.0	208	269	1	0.144	0.535	0.144
ETSOI [169]		8	–	1.5	1.5	90	340	–	0.141	0.62	0.316
CNT FET [320]		9	0	0.65	0.5	94	630	–	0.232	0.184	0.058
CNT FET [51]		5	–	1.05	0.4	207	1412	50	0.162	0.046	0.026
GAA CNT FET	DFT+NEGF	5	0	0.41	0.64	123	1502	0.1	0.084	0.036	0.034
			1			91	1703	0.1	0.063	0.024	0.026
			2			77	1674	0.1	0.057	0.022	0.023
			3			68	1058	0.1	0.050	0.031	0.021
		3	0			349	–	–	0.063	–	–
			1			173	288	0.1	0.038	0.085	0.016
			2			148	1347	0.1	0.035	0.017	0.014
			3			120	1204	0.1	0.037	0.019	0.015
		2	0			392	–	–	0.047	–	–
			1			386	–	–	0.044	–	–
			2			220	80	0.1	0.037	0.297	0.015
			3			153	1129	0.1	0.035	0.020	0.014
		1	3			260	28	0.1	0.021	0.485	0.009

PDP: power dissipation. τ: intrinsic delay time excluding fringe capacitance. *SS*: subthreshold swing. V_{dd}: supply voltage.

12. Summary

12.1. Sub-10 nm 2D FETs

We summarized the main features of the commonly studied semiconductors for the ultra-short transistors in Table 12.1. The scaling behaviors of the on-state current, subthreshold swing, total gate capacitance, effective delay time, and power-delay product of the representative sub-10 nm 2D MOSFETs in the ideal condition from the *ab initio*

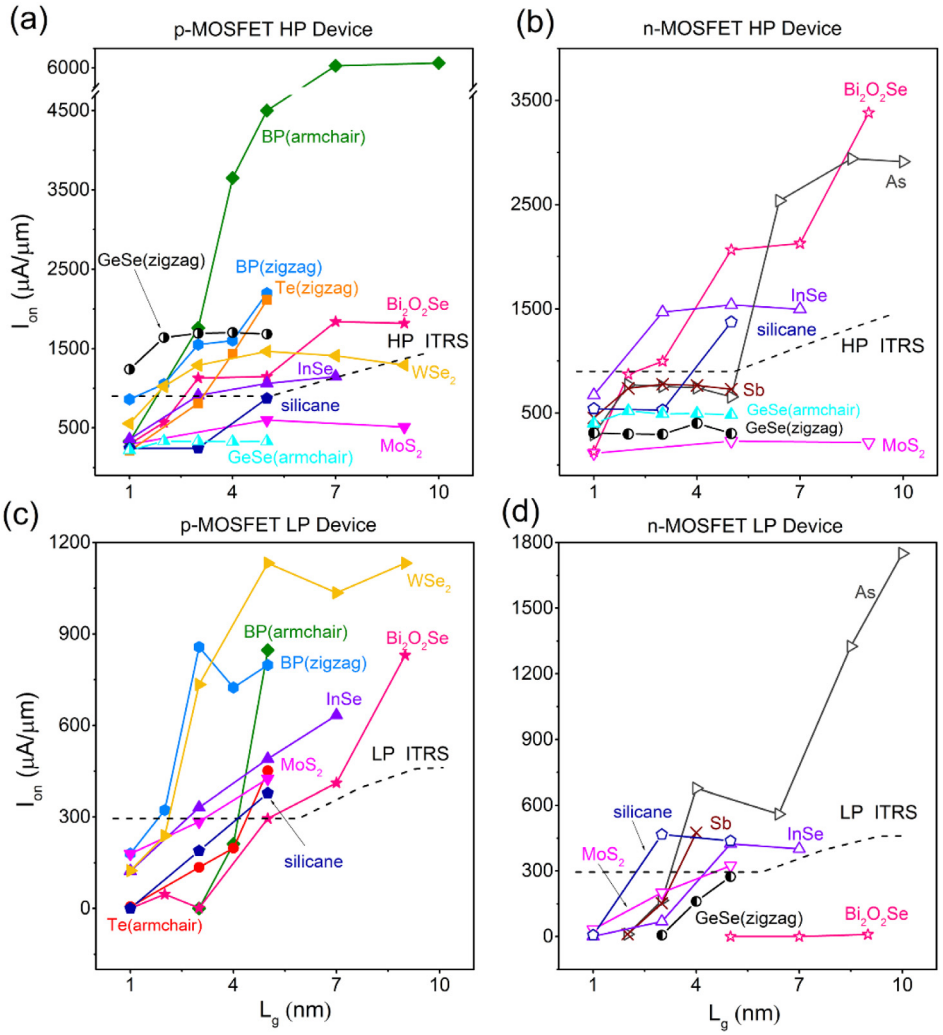


Fig. 12.1. On-state currents of the optimal ML tellerene (Te) [244], ML InSe [227], ML BP [72], ML Bi_2O_2Se [73], ML silicane [166], ML GeSe [214], ML MoS_2 [97], ML WSe_2 [99], ML arsenene (As) [200], and ML antimonene (Sb) [200] MOSFETs at different gate lengths. All the results are based on *ab initio* quantum transport simulations.

quantum transport simulations are shown in Figs. 12.1, 12.2, and 12.3. The on-state currents, total capacitances, and power dissipations generally decrease with the decreasing gate length. The 2D semiconductors generally show strong immunity to the short channel effect. Many of the on-state currents and delay times and almost all the total capacitances and power dissipations of the sub-10 nm ML FETs satisfy the ITRS standard. Armchair ML BP, ML Bi_2O_2Se, ML WSe_2, and ML arsenene lead the on-state current for the *p*-MOSFET HP device, *n*-MOSFET HP device, *p*-MOSFET LP device, and *n*-MOSFET LP device, respectively. The subthreshold swings increase with the decreasing gate length; remarkably, several *SS* values below 60 mV/dec are available. The smallest gate length that meets the ITRS chief requirement can be shortened to 1 nm. Taken the device performance, ambient stability, and experimental accessibility together, ML Bi_2O_2Se, tellurene, WSe_2, silicane, and GeSe appear the most competitive at the present stage.

A small carrier effective mass implies a large carrier effective velocity, favoring a large on-state current; on the other hand, a large carrier effective mass implies a large DOS, also favoring a large on-state current. Fig. 12.4 shows that both a small and large carrier effective mass can lead to a large on-state current for HP and LP devices, and the valley appears at about $m_{\parallel}^{*} \sim 0.8\ m_0$. Unfortunately, the most extensively studied ML MoS_2 performs the most poorly as an HP device. The anisotropic ML phosphorene ($m_{\perp}^{*} \neq m_{\parallel}^{*}$) can simultaneously have a large DOS near the VBM and a large carrier effective velocity along the armchair direction, leading to a relatively high on-state current along the armchair direction.

The calculated EDPs based on 2D MOSFETs [73,97,99,166,244], 1D CNT [354], and UTB Si Fin [170] for the HP and LP applications at $L_g = 5$ nm are benchmarked against the ITRS 2013 version [2] and IRDS 2020 version [6] in Fig. 12.5(a) and (b), respectively. The ideal regions are the lower left corners of the graphs. Due to the slow pace in transistor development

Table 12.1
Summary and comparison of 2D semiconducting materials' properties and electrical performance.

Semiconducting material		E_g (eV)	m_e (m_0)	m_h (m_0)	μ_{FET} ($cm^2 V^{-1}S^{-1}$)	L_g^{min} (nm)	Stability	Ref.
3D bulk	Si	1.12	0.98^l, 0.19^t	0.16^{lh}, 0.49^{hh}	1350–1500 (450–510)	–	Stable	[328–330]
	Ge	0.66	1.64^l, 0.082^t	0.04^{lh} 0.28^{hh}	3900 (1900)	–	Stable	[330–332]
	GaAs	1.4	0.07	0.45	8500 (400)	–	Stable	[330]
2D group IV	Graphene	0	< 0.01	< 0.01	60000	–	Stable	[333,334]
	Graphane	3.5	0.983	0.249	14000	–	Stable	[335,336]
	Nanoporous graphene	1	0.09^l 0.59^t	0.09^l 0.59^t	800 200	–	Stable	[133]
	Graphdiyne	1.1	0.073	0.075	10^4–10^5	–	Stable	[128,139]
	Graphene nanoribbon	0–5	–	–	64–2500	–	Stable	[337]
	Silicene	∼0	< 0.01	< 0.01	∼100	–	Unstable	[42,338]
	ML SiH	1.93 (boat) 2.31 (chair)	0.04	0.076	464	3 (*n*) LP	Stable	[42,166,338]
	ML GeH	2.81	0.09	0.43 (0.1)	30–150	6	Stable	[151,156,173]
2D group V	ML Arsenene	1.76	0.28	–	21 (66)	4 (*n*) LP	Stable	[60,200,206]
	ML Antimonene	1.65	0.28	–	150 (510)	4 (*n*) LP	Stable	[60,200,206]
	ML BP	0.99	–	0.19/3.24 (A/Z)	284 (FLs)	2 (*p*) HP & LP	Unstable	[67,72,339]
	ML BlueP	1.98	0.13 (A/Z)	2.23/1.58 (A/Z)	∼	5.1 (*n*) HP	Unstable	[198,340]
	ML BiH	1.02	0.45	0.16	8.9–12.1	5 (*p*) HP	Stable	[341]
	ML BiN	0.8	0.23	2.00	> 1000	8 (*n*) LP	Stable	[342,343]
	ML AsP	0.92	0.18/1.2 (A/Z)	0.16/1.88 (A/Z)	83 (80–310)	4 (*n*) HP	Unstable	[344–347]
2D group VI	ML Tellurene	1.14	0.83/0.19 (A/Z)	0.11/0.39 (A/Z)	700 (FLs)	4 (*p*) HP & LP	Stable	[31]
2D TMDC	ML MoS_2	1.8	0.51	0.6	∼200	5 (*p*) LP	Stable	[40,65,348]
	ML $MoSe_2$	1.52	0.56	0.66	∼50	–	Stable	[348,349]
	ML WS_2	1.9	0.33	0.43	234	–	Stable	[348]
	ML WSe_2	1.7	0.35	0.45	270	–	Stable	[348]
	ML $MoTe_2$	1.1	0.6	0.71	∼20	–	Stable	[348,350]
2D III–VI	ML InSe	1.52	0.22	3.16	∼1000 (FLs) 240	3 (*p*) HP & LP	Unstable	[226,229]
	ML In_2Se_3	0.86	0.20	0.38	920∼960 (510∼560)	–	Stable	[351]
2D oxide	ML Bi_2O_2Se	1.14	0.2	1.4	∼450 (FLs)	3 (*n* & *p*) HP	Stable	[26,101,257]
	BL Bi_2O_2Se	0.18	0.11	0.81	∼450 (FLs)	5 (*n*) HP	Stable	[101]
Other	ML Sb_2Te_2Se	1.01	0.16/0.12 (A/Z)	0.31/0.36 (A/Z)	∼1000	9 (*n*) HP	Stable	[352]
	ML GeSe	1.1	0.43/0.12 (A/Z)	0.3/0.11 (A/Z)	128.6	1 (*p*) HP	Stable	[214,353]
1D group IV	SW CNT	0.4–0.8	0.1	0.1	∼3000	3 (*n*) HP	Stable	
1D group VI	Te NW	1.09	0.27	0.83	9∼300 (4∼116)	2 (*n*) HP	Stable	[249]

E_g is the bandgap; For anisotropic materials, the effective mass of electron/hole (m_e/m_h) is shown in armchair/zigzag (A/Z) direction, respectively (m_0 is the free-electron mass, and the superscripts *l*, *t*, *lh*, *hh* represent the effective mass of longitudinal, transverse, light hole, heavy hole, respectively.); The electron mobility in a FET (μ_{FET}) is given while the hole mobility is included in the brackets; L_g^{min} is the calculated minimum gate length that meets the ITRS chief requirement (HP or LP) according to the *ab initio* quantum transport simulation, and the polarity (*n* or *p*-type) of the transistor is included in the brackets. FLs: few layers.

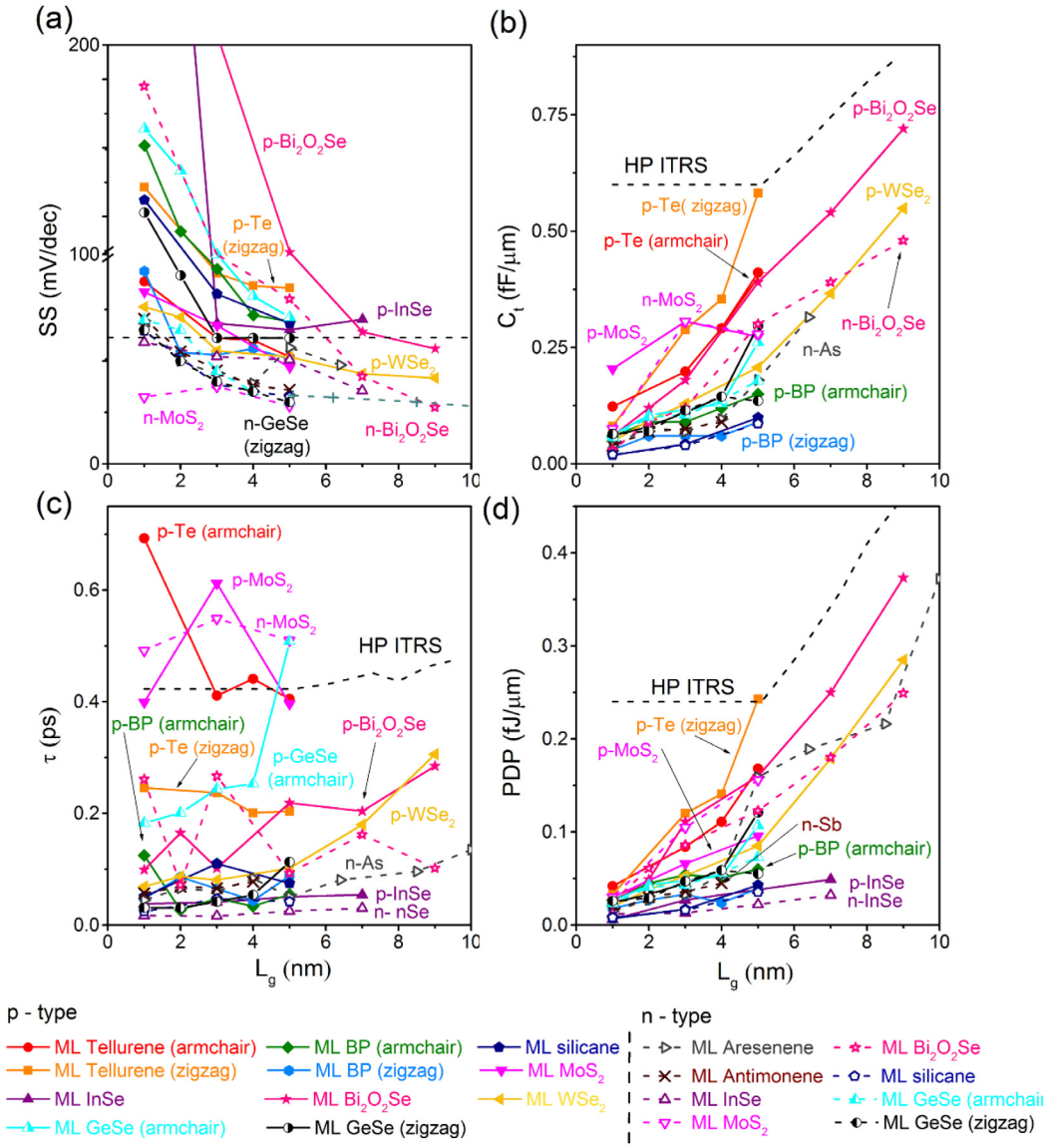


Fig. 12.2. Benchmark of the SS, total gate capacitance (C_g), intrinsic delay time (τ), and PDP of the sub-10 nm 2D MOSFETs against the HP requirements of ITRS 2013 (black dashed line). V_{dd} = 0.64–0.72 V [72,97,99,166,200,214,244].

in recent years, the EDP standard is amended less aggressively in the IRDS 2020 than the ITRS 2013 version. All the EDPs of the checked HP and LP MOSFETs satisfy the requirement of the IRDS 2020 version until the 2031 horizon. The given MOSFETs also meet the requirements of the ITRS 2013 version from 2020 to 2028 horizon except for the ML HP MoS_2 MOSFET [97]. Among the HP devices, the ML InSe has the smallest EDP, followed by 1D CNT [354], ML silicane [166], and UTB Si Fin [170]. Among the LP devices, the ML silicane has the smallest EDP, followed by ML InSe and ML Tellurene [227,244]. Unfortunately, the widely studied ML MoS_2 has the most inferior performance in the HP application and mediocre performance in the LP application [97].

Most of the quantum transport simulation results in the above are calculated in the optimistic condition in terms of geometry, transistor without defects, ballistic transport, and Ohmic contact despite the inclusion of the fringing capacitance. Therefore, they show the performance limit of the devices. We should give up the 2D MOSFETs that cannot meet the ITRS requirement even in the ideal condition. At the same time, those 2D MOSFETs with competitive properties deserve further development.

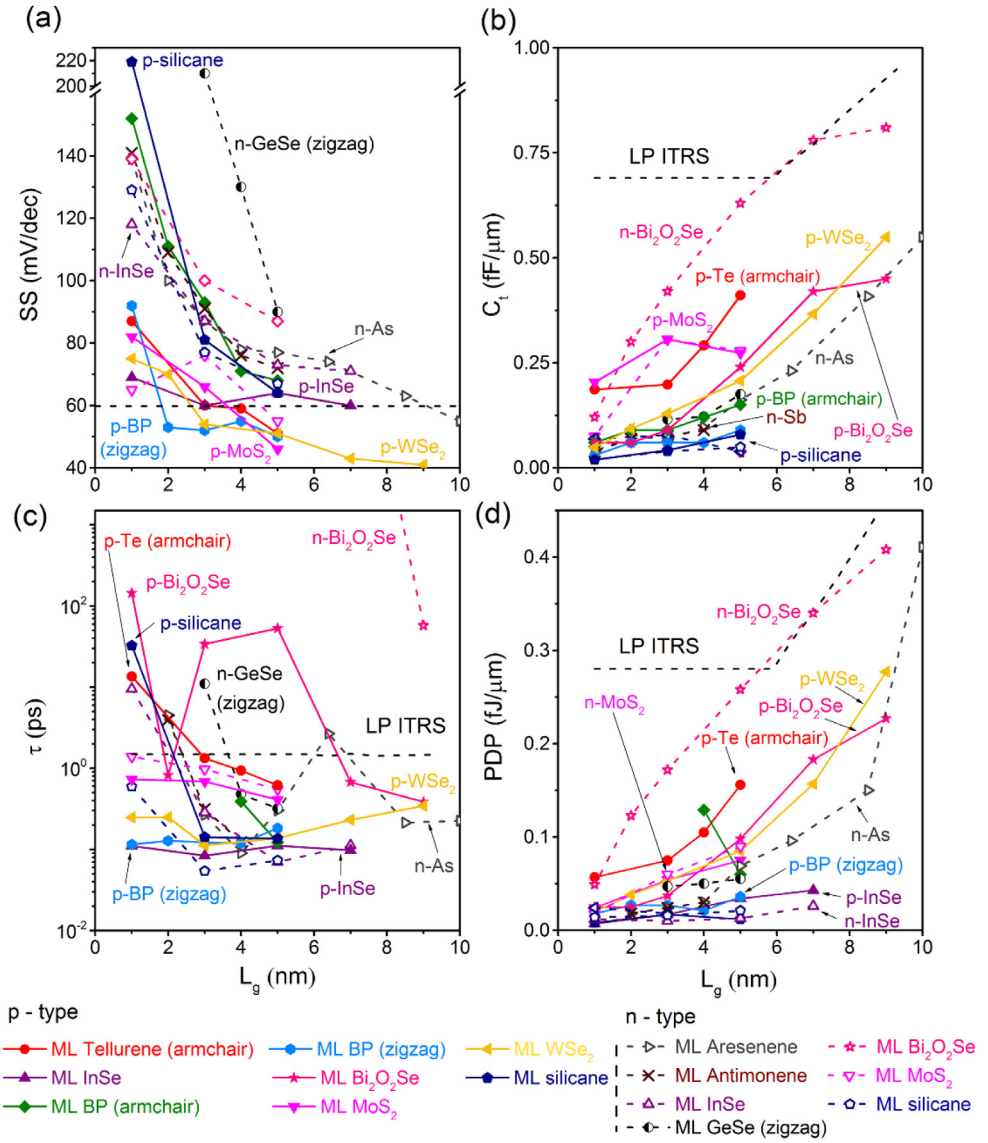


Fig. 12.3. Benchmark of the SS, total gate capacitance (C_g), intrinsic delay time (τ), and PDP of the sub-10 nm 2D MOSFETs against the LP requirements of ITRS 2013 (black dashed line). V_{dd} = 0.64–0.72 V [72,97,99,166,200,214,227,244].

12.2. Sub-10 nm CNTs vs. 2D FETs

1D CNT and 2D materials both have excellent gate efficiency due to their atomic body [9–11]. However, the mobility of CNT can exceed 3000 $cm^2/V\cdot s$ at room temperature [313,319,355], higher than most 2D semiconductors. For the sub-10 nm gate-length region where quasi-ballistic transport dominates, saturation velocity is a more critical parameter than mobility, a key parameter for diffusive transport. CNT with a diameter of 1–2 nm has a small effective mass ($\sim 0.1m_0^*$) and its unidirectional thermal velocity is 4×10^7 cm/s [356,357], which is much higher than the saturation velocity (v_{sat}) of most 2D materials, such as TMDs (5×10^6 cm/s) and X-enes (5×10^7 cm/s) [4]. This high v_{sat} of CNT makes it have the possibility to provide a high on-state current. Experimentally and theoretically, the CNT FET with 5 nm gate length exhibits high on-state currents of 1412 and 1775 μA/μm under a small bias of 0.4 V, respectively (normalized by assuming 200 CNTs per micrometer) (Table 12.2). However, CNT has a relatively small bandgap (0.4–0.8 eV), resulting in the ambipolar transport deteriorating the off-state performance and making it hard to be applicable in LP implementations. The *ab initio* quantum transport simulations also demonstrated that the LP off-state target is hard to reach due to CNT's relatively low effective mass [321,333]. By contrast, most of the 2D materials can meet the needs of the HP and LP application.

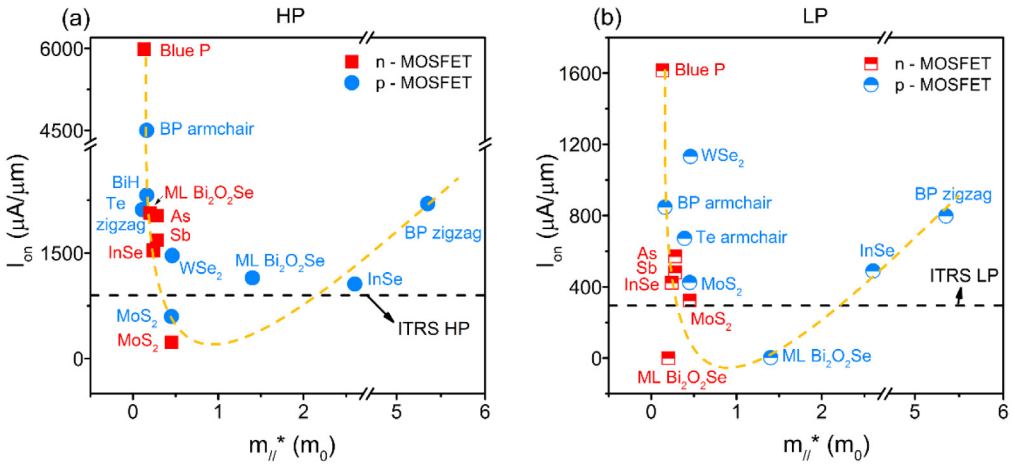


Fig. 12.4. On-state current for the HP (a) and LP (b) applications of the *p*- and *n*-MOSFETs as a function of the ML material effective mass m^* [72,97,99,166,200,214,227,244]. The dashed yellow curve is a guide for the eyes.

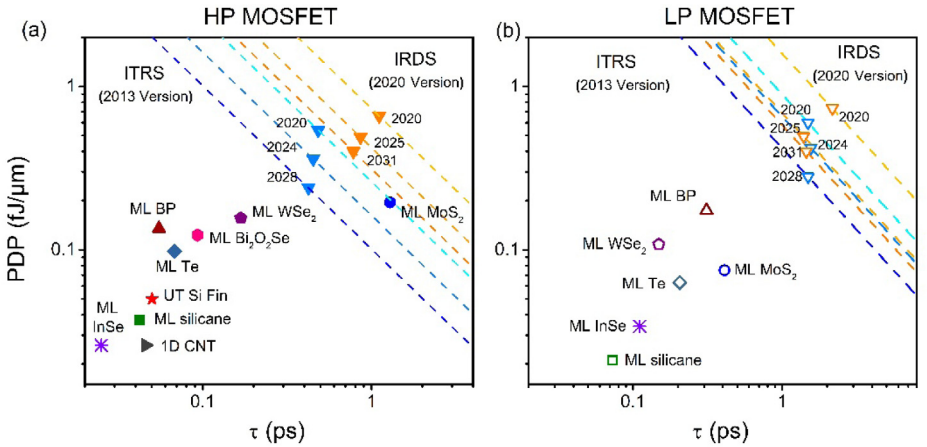


Fig. 12.5. Benchmark of the calculated power dissipation as a function of delay time for the HP (a) and LP(b) devices of different MOSFETs at L_g = 5 nm [72,97,99,166,200,214,227,244] against the ITRS 2013 (blue dots) and IRDS 2020 (orange dots) [2,6]. The dashed lines represent the equation: EDP = PDP×τ.

Besides, the easy stacking in the vertical direction due to interlayer vdW interaction in 2D materials makes the new implementation of heterostructure devices possible [36].

It is hard to control the chirality of the CNTs precisely, but many signs of progress have been made in synthesizing all-semiconducting CNT, including CVD growth and solution-based purification [358–364]. Though facing enormous challenges, researchers have developed CNT based computers comprising from 178 to >14000 CNT FETs based on CVD and purified CNT solution technology, respectively, that is, from 1 bit to 16 bit operation, and this shows the prospect of CNT commercial application in beyond-Si microprocessors [365,366]. For 2D materials, devices are mostly fabricated from exfoliated samples. Though exfoliated layers bring high electrical performance, wafer-scale and high-quality growth methods are desired for ultra-large ICs applications. Progress has been made successively, such as the growth of foot-long single-crystal graphene [367], a 100-square-centimeter single-crystal hexagonal boron nitride ML [368], and the large-area uniform growth of MoS_2 by CVD [92]. And then, the first 1 bit MoS_2 CPU consisting of 115 transistors was fabricated based on the CVD-grown large-area BL MoS_2 uniform films [95]. Overall, material preparation with high quality is vital because it can effectively promote ICs and industrial applications.

12.3. Sub-10 nm 2D TFETs vs. 2D MOSFETs

We compare I_{on} (for HP application) and *SS* between the 2D ML planar HomJ TFETs and the 2D ML MOSFETs as a function of the bandgap and effective mass [6,91,97,166,170,227,324] in Fig. 12.6. Another critical factor, *i.e.*, anisotropic electronic property, that makes an advantage for both the TFET and MOSFET, is not discussed here. The I_{on}(HP) of the

Table 12.2
Comparison of the experimental and theoretical on-state current I_{on} (in the unit of μA/μm) of the sub-10 nm CNT and ML 2D FETs. The working voltage is 0.4 V for the CNT FET in both the simulation and experiment, and it is 0.64 V for the simulated ML Te, InSe, WSe_2, Sb, and MoS_2 FETs, 0.75 V for the simulated ML BP and As FETs, 0.72 V for the simulated ML Bi_2O_2Se FET, and 1 V for the ML MoS_2 FET in the experiment.

	CNT [51]	BP [72,199]	As [60]	Te [244]	Bi_2O_2Se [73]	InSe [227]	WSe_2 [99]	Sb [60]	MoS_2 [97]
Experimental data	1412	–	–	–	–	–	–	–	250
Simulation for HP	1775	6025	2941	2114	1838	1538	1464	775	519
Simulation for LP	–	857	677	451	830	424	1131	475	324

checked 2D MOSFETs are always higher than their 2D planar TFET counterparts though the 2D TFETs generally have lower *SS*.

The optimal E_g range to surpass the ITRS requirements for the HP devices is 0.87∼1.09 eV in the 2D ML TFETs. Whereas in the 2D ML MOSFETs, there is no apparent optimal range of E_g (Fig. 12.6(a)). The desired effective mass for the HP devices is also rigorous in the 2D ML TFETs. Both electron and hole effective masses affect the 2D ML TFET, and a relatively narrow $\sqrt{m_e \cdot m_h}$ range of 0.12 ∼0.14 m_0 is suggested for the 2D ML TFET to surpass the ITRS HP device. While for the 2D ML MOSFET, a sole electron/hole effective mass is required for the *n*-/*p*-type device, and the optimal range of $m_{e/h}$ is much broader, *i.e.*, either small (< 0.46 m_0) or large $m_{e/h}$ (> 0.81 m_0) is favored for the HP devices (Fig. 12.6(b)).

As anticipated, *SS* of the most checked 2D ML TFETs break the room-temperature Boltzmann thermionic limit of 60 mV/dec due to the band-to-band tunneling mechanism, and the lowest reported *SS* is only 30 mV/dec. For the 2D ML MOSFETs, sub-60 mV/dec *SS* can also achieve because of the unneglectable intra-band tunneling current, and the lowest reported *SS* is 55 mV/dec. It is fanciful to see that both the optimal E_g and effective mass ranges for *SS* are almost reversed to I_{on}. That is to say, the HP device with a larger I_{on} probably also has a larger *SS*. The optimal E_g range for the sub-thermionic *SS* is 0.9∼1.75 eV in the 2D ML planar TFETs and 1.14∼1.9 eV in the 2D ML MOSFETs (Fig. 12.6(c)). The optimal $\sqrt{m_e \cdot m_h}$ range is 0.13∼0.35 m_0 in the 2D ML TFET, and the optimal $m_{e/h}$ range is 0.2∼0.6 m_0 (Fig. 12.6(d)).

The calculated EDPs of the 2D ML planar HomJ TFETs for the HP and LP applications at $L_g = 10$ nm are benchmarked against the ITRS 2013 version [2] (from 2020 to 2028) and IRDS 2020 version [6] (from 2020 to 2031) in Fig. 12.7(a) and (b), respectively. All the EDPs of the HP and LP 2D ML planar HomJ TFETs satisfy the listed requirements of the ITRS 2013 and IRDS 2020. Among the EDPs of the HP ML planar HomJ TFETs in Fig. 12.7(a), the ML bismuthene and ML GeSe planar HomJ TFETs are ranked the smallest No.1 and 2, respectively [305,369]. Among the LP 2D devices in Fig. 12.7(b), the EDP values of the ML GeSe and ML BP planar HomJ TFETs are the smallest No.1 and 2, respectively [282,284,369]. The EDPs of the 2D ML planar HomJ TFETs that satisfy both the ITRS HP and LP criteria decrease in the order of GeSe > BP > SnSe > Sb > As > WTe_2 [215,285,305,369].

The EDPs of the different 2D ML MOSFETs and ML planar HomJ TFETs for the HP and LP applications are compared in Fig. 12.8(a) and (b), respectively. Remarkably, the 2D ML planar HomJ TFETs always show smaller EDPs than their 2D ML MOSFET counterparts regardless of the HP or the LP application. For the HP devices, the EDPs of the 5 nm-L_g ML BP planar HomJ TFET [284], the 10 nm-L_g ML arsenene planar HomJ TFET [305], and the 5 nm-L_g ML GeSe planar HomJ TFET [369] are only 1/3, 1/5, and 1/10 of their MOSFET counterparts, respectively [60,72,200,214]. For the LP devices, the advantage of the 2D ML planar HomJ TFET over the MOSFET counterpart is even more prominent. The EDPs of the 10 nm-L_g ML arsenene planar HomJ TFET [305] and the 5 nm-L_g ML BP planar HomJ TFET [284] are only 1/10, 1/30 of their MOSFET counterparts, respectively [72,200]. Besides, both the PDP and τ of the 5 nm-L_g LP ML BP planar HomJ TFET, the 5 nm-L_g HP ML GeSe planar HomJ TFET, and the 10 nm-L_g ML arsenene planar HomJ TFET are significantly smaller than those of their MOSFET counterparts. Hence, these three 2D planar HomJ TFETs are superior to their MOSFET counterparts in the power dissipation and delay two chief figures of merit.

13. Challenge and opportunity

Because of flat surfaces, atomic thickness, and easy stacking in the vertical direction, 2D semiconductors are predicted to be promising materials in shrinking transistors and extending Moore's law. It is too early to conclude whether 2D FETs will replace the 3D silicon techniques in the ultra-scale. However, 2D FETs will undoubtedly play a key role. Many efforts have been put into this area, and eye-catching progress has also been made. However, to realize the large-scale integrated circuit out of the sub-10 nm 2D transistors, there are still many inevitable challenges that must be handled.

(1) How to grow large single crystals of high quality? In the current stage, the devices are mostly fabricated from exfoliated 2D material samples. While these exfoliated layers render high device performance, more scalable and reliable synthetic methods are desired for the industrial application of 2D materials. The growth of foot-long single-crystal graphene on polycrystalline substrates has been reported [367]. Liu et al. successfully synthesized a 100-square-centimeter single-crystal hexagonal boron nitride monolayer on copper by annealing regular industrially produced copper foils [368] (Fig. 13.1). Other methods such as self-collimated grain formation have also been invented to grow large single-crystal hexagonal boron nitride film [370]. Very recently, Ye et al. synthesized wafer-scale single-crystalline $MoTe_2$ through a novel seeded 2D epitaxy technique [371]. This technique alleviates the problem of translational grain boundaries in the 2D film and derives crystalline with excellent uniformity. Transistor arrays fabricated by the 2H-$MoTe_2$ single-crystal

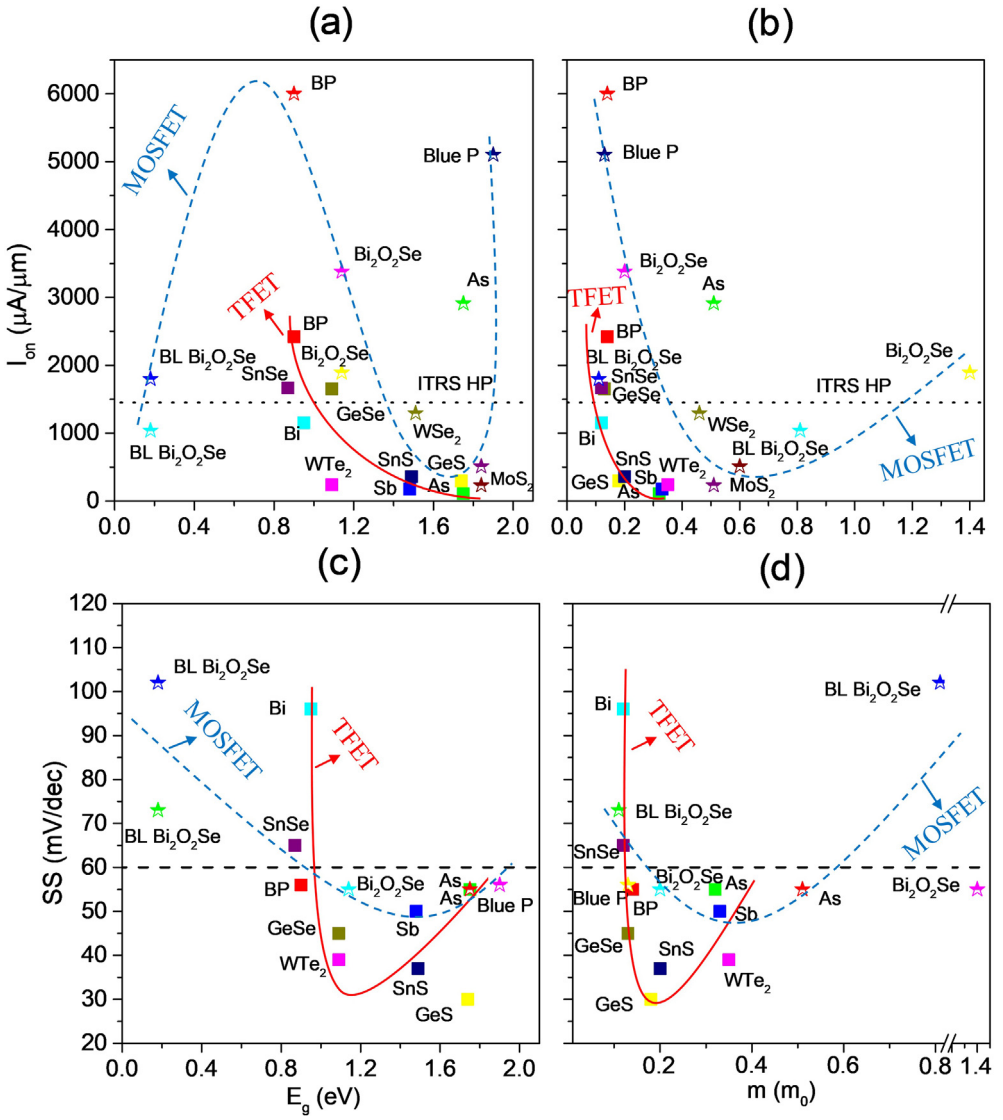


Fig. 12.6. Comparison of I_{on} (for the HP application) (a–b) and *SS* (c–d) between the 2D ML planar HomJ TFETs and 2D ML MOSFETs with a homogeneous planar channel as a function of the (a, c) bandgap and (b, d) effective mass of the ML channel material (with one exception of BL Bi_2OSe_2) along the transport direction [99,101,182,198,199,283]. Here, $L_g = 9\sim10$ nm, $V_{dd} = 0.72\sim0.74$ V, and $I_{off} = 0.1$ μA/μm. The effective mass is an average effective mass of hole and electron $\sqrt{m_e \cdot m_h}$ for a TFET, and a sole hole or electron effective mass for a MOSFET. All the data are calculated at the *ab initio* level. The solid squares and half-filled stars stand for the 2D ML TFETs and MOSFETs, respectively. The red and blue dash lines are guides to the eyes.

display high electrical performance with 100% device yield [371]. We anticipate the synthesis of other 2D materials (such as MoS_2 and phosphorene) with high quality and large size by adopting these related approaches.

(2) How to predict and assess the device performance of the sub-10 nm more accurately? The predicted device performance from most of the current *ab initio* quantum transport simulations is in the ideal condition (perfect geometry, ballistic transport, and Ohmic contact). The defects, impurity, and phonon scattering have not been fully considered in most of these *ab initio* simulations. Besides, the *ab initio* quantum transport simulations usually apply the degenerately doped channel materials as the electrode, and thus the electrode/channel contact is Ohmic. However actually, bulk metal is often used as the electrodes because the controllable substitutional doping of 2D materials remains difficult in experiments. A Schottky barrier commonly exists at the metal/2D semiconductor interface and hinders the carrier injection. *Ab initio* quantum transport simulations with the inclusion of the dissipative transport and Schottky barrier

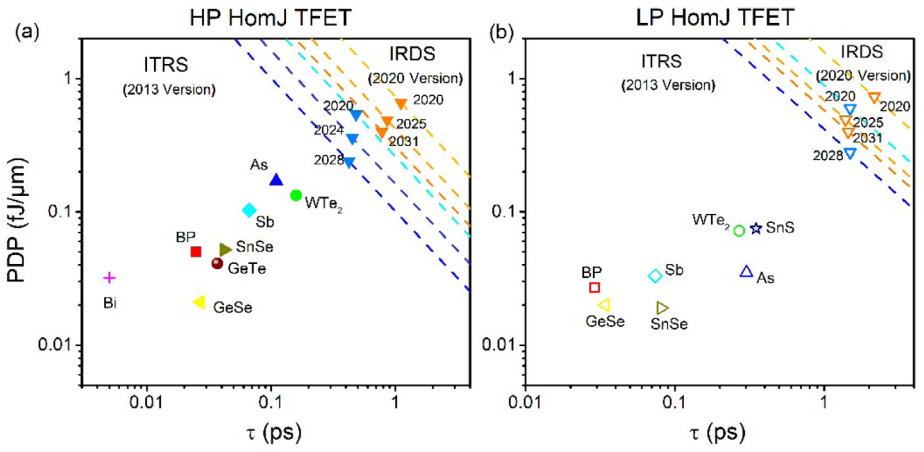


Fig. 12.7. Benchmark of the calculated power dissipation as a function of delay time for the HP (a) and LP(b) devices of different 2D ML planar HomJ TFETs at L_g = 10 nm [215,282–285,305,369] against the ITRS 2013 [2] (blue dots) and IRDS 2020 [6] (orange dots). The dashed lines represent the equation: EDP = PDP×τ.

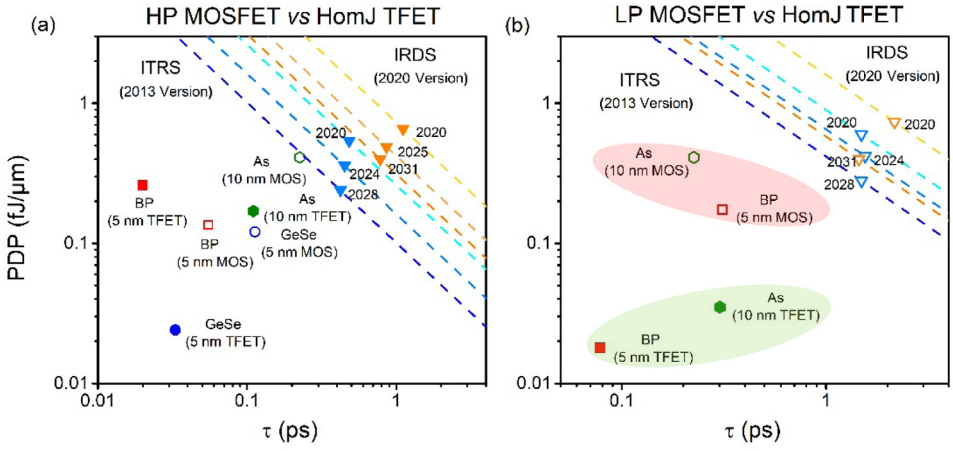


Fig. 12.8. Comparison of the calculated EDP between the 2D ML planar HomJ TFETs and ML MOSFETs for the HP(a) and LP(b) devices [282,284,305, 369]. EDP standards from the ITRS 2013 (blue dots)/IRDS 2020 (orange dots) are also shown [2,6]. The dashed lines represent the equation: EDP = PDP×τ.

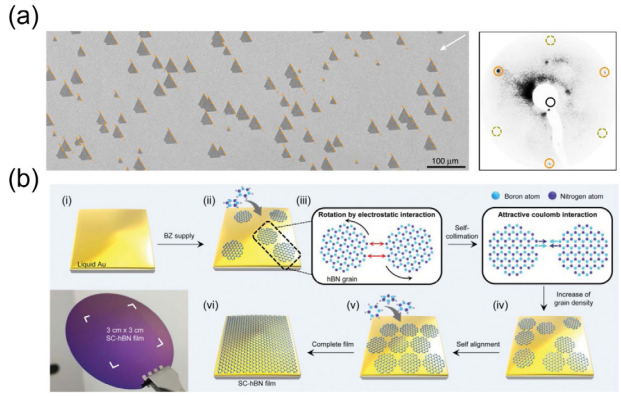


Fig. 13.1. Fabrication of large-scale single-crystal h-BN layers. (a) SEM image and Representative LEED pattern of as-grown unidirectionally aligned hBN domains on the Cu (110) [368]. (b) Schematic illustration for the growth of single-crystal hBN film by means of self-collimated grain formation and a photograph of a wafer-scale single-crystal h-BN film on a SiO_2-Si wafer [370].
Source: (a) is reproduced from Ref. [368]. (b) is reproduced from Ref. [370].

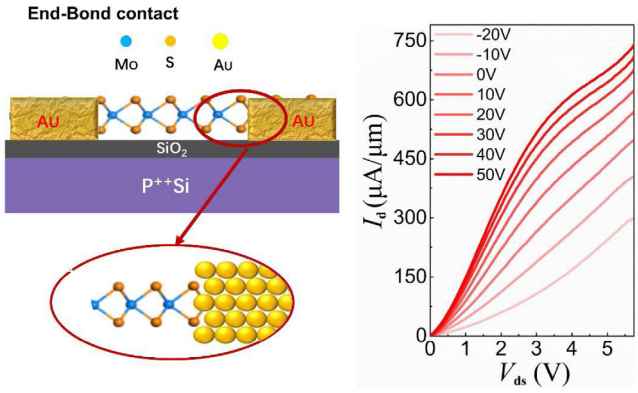


Fig. 13.2. A clean end-bond contact scheme that leads to an ultralow contact resistance of 2.5 kω · μm and a record saturation current of 730 μA/μm at 300 K.
Source: Reproduced from Ref. [372].

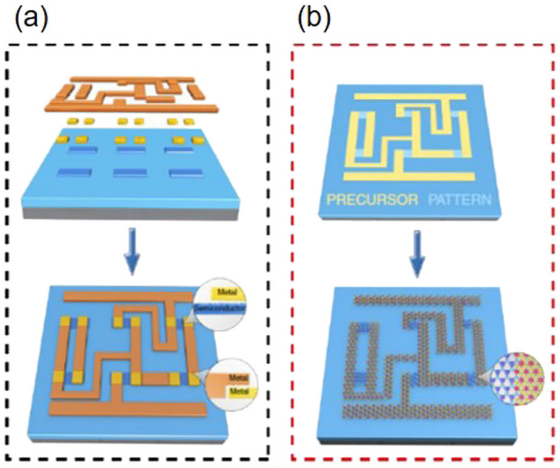


Fig. 13.3. (a) Conventional circuit fabrication featured by step-by-step construction of the channels, contacts, and interconnects and a further connection of the components physically with interfaces. (b) Scheme proposed by Jiao et al. for constructing ultrathin circuits by simultaneously synthesizing and integrating electronic components [50]. Precursors are first patterned into expected structures according to the device design, followed by one-step phase-controlled chemical synthesis. The predesigned precursor pattern is converted into an integrated circuit where the semiconducting phase serves as channels and the metallic phase as source–drain electrodes and interconnects. All these components are connected via strong covalent bonds.
Source: Reproduced from Ref. [50].

effects will undoubtedly lead to a more accurate result. However, the 2D FETs that perform poorly even in the ideal condition probably should be given up. By contrast, those that can meet the ITRS merit need further consideration.

(3) How to improve the contacts in the 2D semiconductor-based transistors? From the device perspective, the interfaces involved in a 2D material-based transistor, including channel–electrode, channel–dielectrics, and channel–substrate, require careful engineering [46,373]. Though the 2D materials-based transistors have already been scaled down to 4 nm channel length [46] or 1 nm gate length [49], the on-state current appears much smaller than the silicon counterparts. One major cause is the non-ideal interfaces that severely degrade the device performance and impede intrinsic 2D semiconductors' excellent properties. In the sub-10 nm regime, these effects from the interfaces are expected to be even more apparent. A few innovative approaches have been introduced to improve the electrical contacts, such as using 2D metals (graphene, metallic $NbSe_2$, and MXene) as electrodes [46,88,373–378], phase engineering of the 1T-2H or 1T′-2H TMDCs contacts with sharp atomistic scale interface [87,94], and inserting tunnel layer between the bulk metal and 2D semiconductors [379]. With a clean end-bond Au contact (Fig. 13.2), a record saturation current density of 730 μA/μm in the ML MoS_2 transistor is observed [372].

(4) How to integrate individual 2D devices into circuits? After making sure of a single transistor's performance, the next step should be the transistors' large-scale integration at a circuit level. A microprocessor-based on the MoS_2 layers has been realized in 2017 [95]. However, the conventional step-by-step device fabrication processes often introduce defects and impurities, which will lead to the degradation of the device performance. Therefore, it is highly desirable

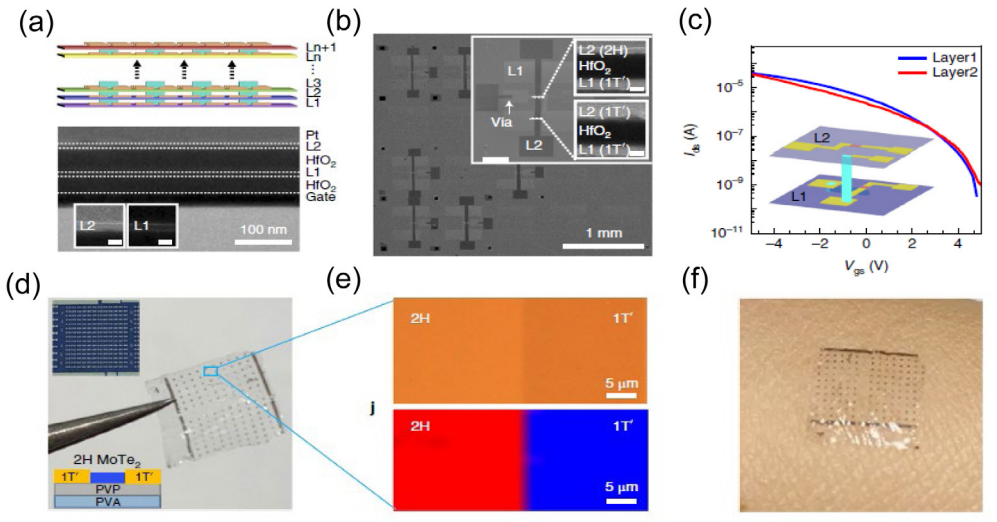


Fig. 13.4. (a) Schematic illustration of a 3D integrated circuit fabricated by the repeated growth of phase-patterned $MoTe_2$ and cross-sectional TEM image of the multilayered structure in a bilayer $MoTe_2$ circuit. Inset: zoomed-in images of the first (L1) and second (L2) $MoTe_2$ layers. (b) SEM image of $MoTe_2$ device arrays on the L1 and L2. Inset: two vertically connected devices in adjacent layers. (c) Transfer characteristics of the two connected neighboring devices. Inset: schematic 3D illustration of the device layout. The 1T′ $MoTe_2$ in L1 serves as the gate of the devices in L2. (d) Self-supporting PVP/PVA film with an array of 144 stretchable $MoTe_2$ transistors. Insets: device array on a SiO_2/Si substrate before peeling-off (top) and cross-sectional schematics for the film with devices (bottom). (e) Optical and Raman mapping image of a 1T′/2H $MoTe_2$ junction on PVP/PVA film, respectively. (f) Chemically synthesized $MoTe_2$ devices on PVP/PVA film adhering to a human wrist.
Source: Reproduced from Ref. [50].

to design new device manufacturing strategies, particularly for 2D semiconductors. Via a one-step chemical approach, Jiao et al. synthesize and integrate simultaneously ultrathin channels, contacts, and interconnects in the phase-patterned 2D $MoTe_2$ [50] (Fig. 13.3). This construction strategy effectively prevents interfacial contamination and is promising for those 2D semiconductors with both metallic and semiconducting phases.

Overcoming these challenges will bring out other new opportunities for 2D FETs, including high-density data handling, wearable electronics, and multifunctional electronics.

(1) Compared with bulk silicon, whose surface has many dangling bonds and is uneven, the ultrathin, flat, and dangling-bond-free nature of 2D materials enables the maximization of the vertical integration density and the realization of the high-quality, sharp interfaces with few trap states. To realize 3D integration of the FETs, Jiao et al. synthesized a layer of $MoTe_2$ with 2H/1T′ phase patterns on a SiO_2/Si substrate and then covered it with a thin film of HfO_2 [50]. Via the same procedures, an extra patterned 2H/1T′ $MoTe_2$ layer was produced on the HfO_2 film (Fig. 13.4(a–c)). Arrays of the $MoTe_2$ FETs were successfully fabricated on different levels and exhibited similar *p*-type switching mode and excellent on/off current ratios of about 10^5.

(2) Owing to good flexibility, the atomically thin 2D semiconductors also serve as ideal candidates for fabricating flexible, stretchable, and wearable electronic devices. A free-standing thin polyvinylpyrrolidone and polyvinyl alcohol film of the chemically synthesized $MoTe_2$logic device arrays were successfully peeled off from the original substrate (Fig. 13.4(d–f)). The thin film was conformably stuck to the skin and sustained a tensile strain of up to 14%.

(3) In the sub-10 nm region, electron–phonon interaction remains for a conventional semiconductor channel, although its effect on the on-state current is small. The concept of topological transistors has attached much attention in recent years [4,380,382–387]. In an on-state, spin and charge flow without dissipation in topological preserved edge states, which is crucial to create low-power devices [85,388]. In an off-state, the channel turns to be an insulator without conducting channels. The electric-field-induced topological phase transition is necessary to switch topological transistors between on and off-states. The transition has been predicted in some topological insulators, such as a thin film of Na_3Bi [385], Cd_3As_2 [385], SnTe [386], Pb_{1-x} Sn_xSe (Te) [386], and monolayer (ML) 1T′-MX_2 (M = (tungsten or molybdenum) and X = (tellurium, selenium, or sulfur)) [382]. Luckily, an electric-field-induced topological phase transition has been realized experimentally in ML and BL Na_3Bi [380] (Fig. 13.5(a, b)). The ML/BL Na_3Bi is a 2D topological insulator, namely the quantum spin Hall insulator (QSH). The bulk bandgap of ML Na_3Bi is completely closed and reopened as a trivial insulator with the increasing electric field (Fig. 13.5(c)). The maximum bandgap of the trivial insulator is up to 90 meV, much larger than the thermal energy at room temperature (23 meV). The electric-field-induced topological phase transition and the large trivial bandgap make ML Na_3Bi a competitive material in fabricating room-temperature topological transistors. Recently, a first-principles quantum transport simulation of an ultrashort topological transistor based on the topological insulating ML Na_3Bi zigzag nanoribbon (ZNR) is performed, and an on/off ratio of 4 71 and a large I_{on} = 1090 μA/μm is obtained [381] (Fig. 13.5(d)). Although topological transistors have not been realized yet, the fabrication of topological transistors would be quite promising based on the experimental progress.

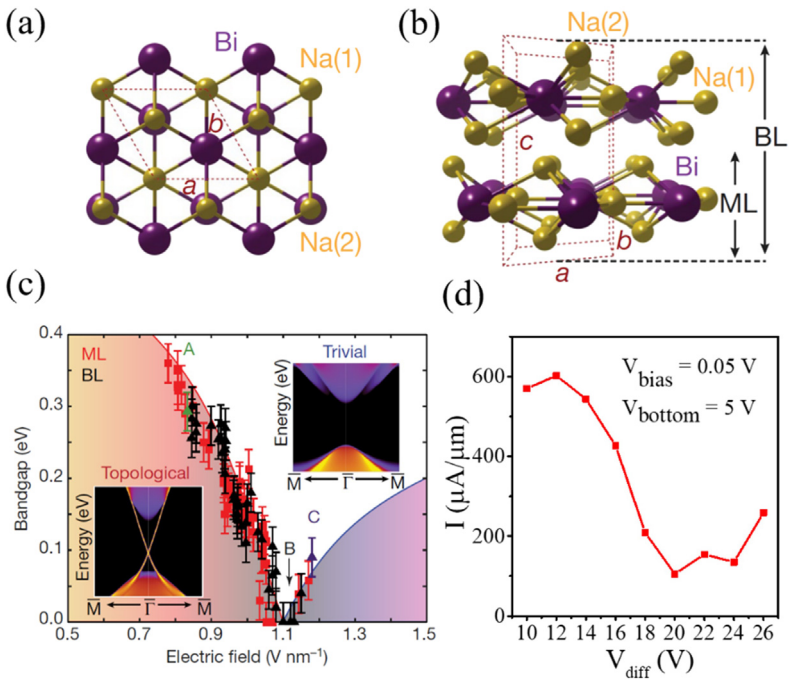


Fig. 13.5. (a) Top view of the ML Na_3Bi. (b) Side view of the ML and BL Na_3Bi. The dashed line represents the unit cell of ML (a) and bulk (b) Na_3Bi, where $a = b = 0.545$ nm and $c = 0.965$ nm. (c) Bandgap obtained from dI/dV spectra under different electric fields for ML (red squares) and BL (black triangles) Na_3Bi, orange and purple shaded regions represent guides to the eye. Insets represent DFT projected edge state band structures below and above the critical field, where the color represents the spectra weight. (d) Characteristic of the ML Na_3Bi nanoribbon topological transistor with $L_g = 2.7$ nm. The black/blue circles represent the on-state/off-state, respectively. $V_{top}/V_{bottom}/V_{bias}$ represents the voltage of the top/bottom gate and the bias, respectively. $V_{diff} = V_{top} - V_{bottom}$.
Source: Reproduced from Ref. [380] and Ref. [381].

14. Conclusion

In the ideal conditions, many representative 2D MOSFETs (*i.e.*, phosphorene, silicane, tellurene, arsenene, WSe_2, InSe, Bi_2O_2Se, GeSe, *etc.*) in the ML limit show excellent device performance (in terms of on-state current, delay, and power dissipation) in the sub-10 nm gate-length region and have the potential to extend Moore's law down to 1–2 nm physical gate length for both the HP and LP applications according to the *ab initio* quantum transport simulations. The use of the negative capacitance technique can further improve the device performance. The experimental 1D CNT FETs outperforms the actual Si FinFETs in the sub-10 nm region, and their device performance is well reproduced by the *ab initio* quantum transport simulation. The theoretical device performance of the sub-10 nm MOSFETs based on 1D CNT and excellent 2DSCs is at the same level. Therefore, the predicted high-performance sub-10 nm 2D MOSFETs are highly promising as long as a low-resistance contact, preferably Ohmic contact, can be realized, although, at present, the actual sub-10 nm 2D FETs are less satisfactory. Compared with the 2D MOSFET counterparts, the sub-10 nm 2D TFETs generally own smaller EDP in theory and appear especially suitable for the LP applications, and the 2D HetJ TFETs generally exceed the 2D HomJ FETs. Both a very small and a very large carrier effective mass favor the 2D MOSFETs, but only a small carrier effective mass is preferred by the 2D TFETs.

Note added in proof:

After acceptance of this work, we became aware of two recent experimental studies on the ML MoS_2 [389] and BL WSe_2 transistors [390] by Kong *et al.* and Duan *et al.* Ohmic contact is realized by utilizing semimetal Bi electrode or metallic VSe_2 vdW electrodes, respectively. The resulting maximum currents (or saturation currents) of the ML MoS_2 and BL WSe_2 FETs have reached very high values of 1135 and 900 μA/μm, respectively [389,390]. These current values approach the maximum currents (or saturation current) of about 1500 μA/μm predicted for the ML MoS_2 SBFET and ML WSe_2 MOSFET models based on *ab initio* quantum transport simulation [96,99].

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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